

Fig. 1

Fig. 2

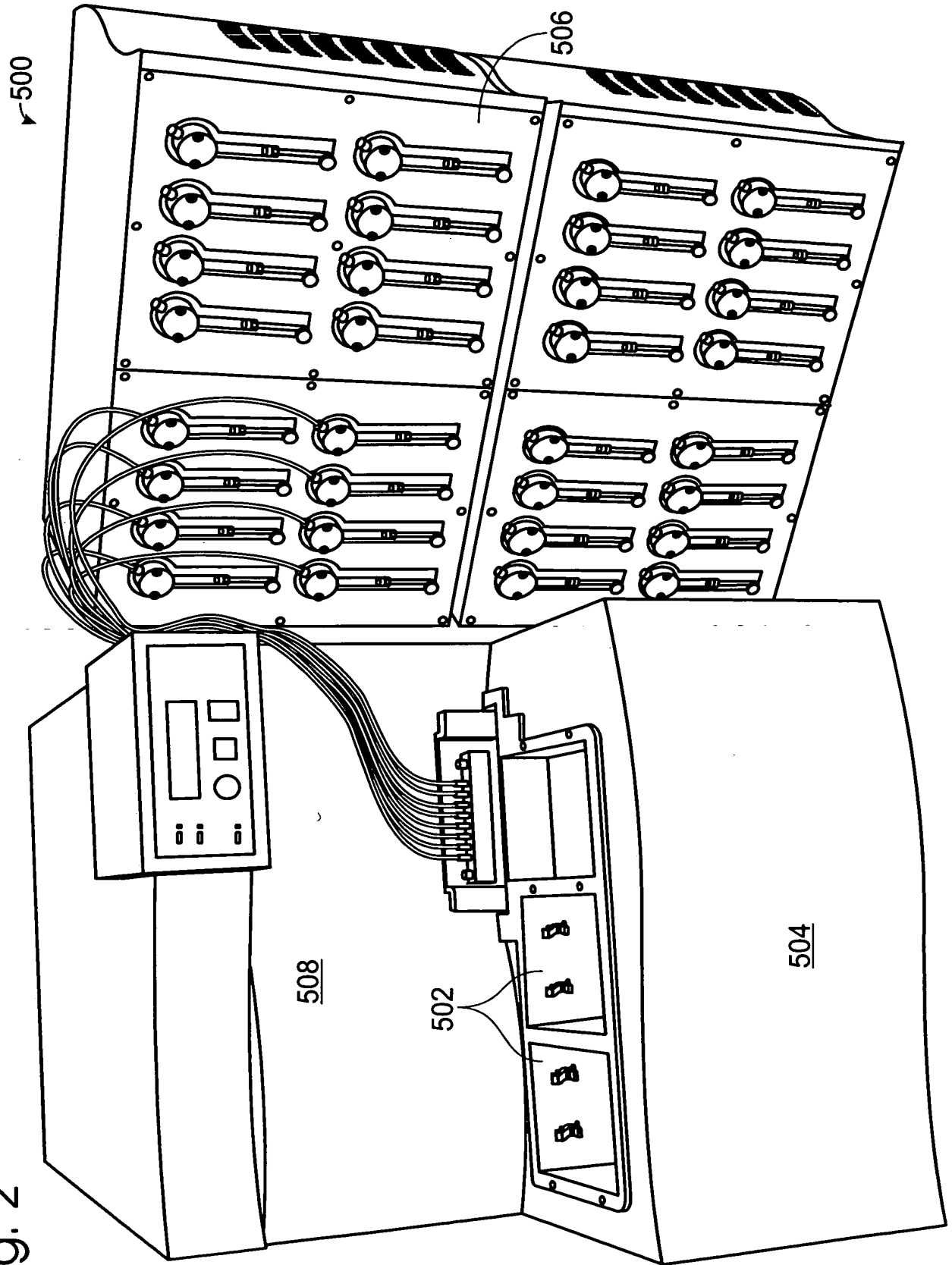


FIG. 2

Fig. 3

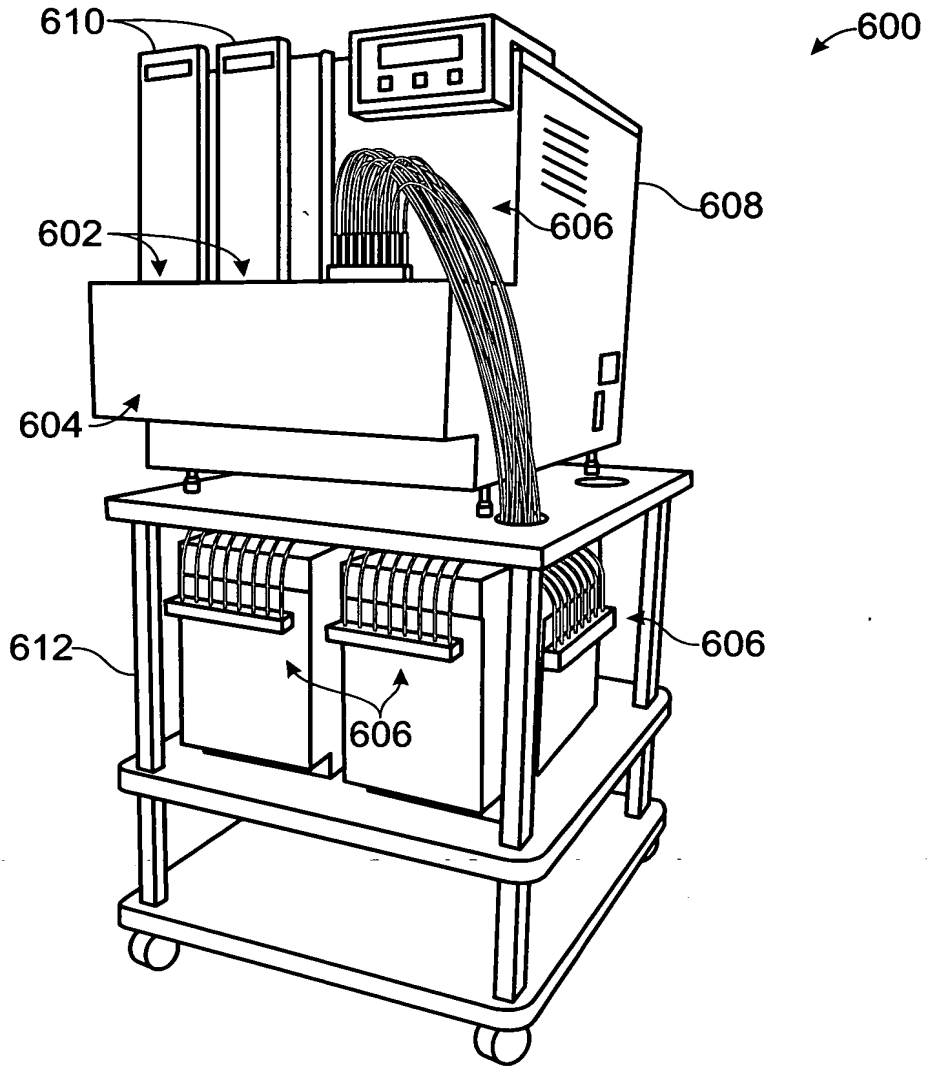
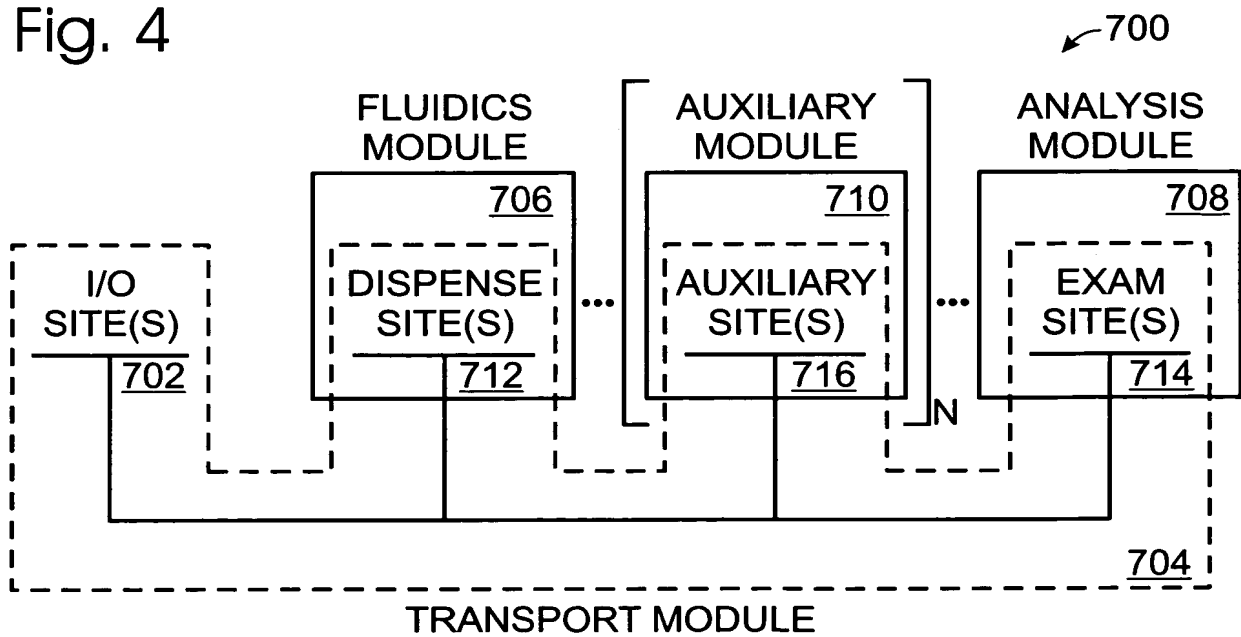
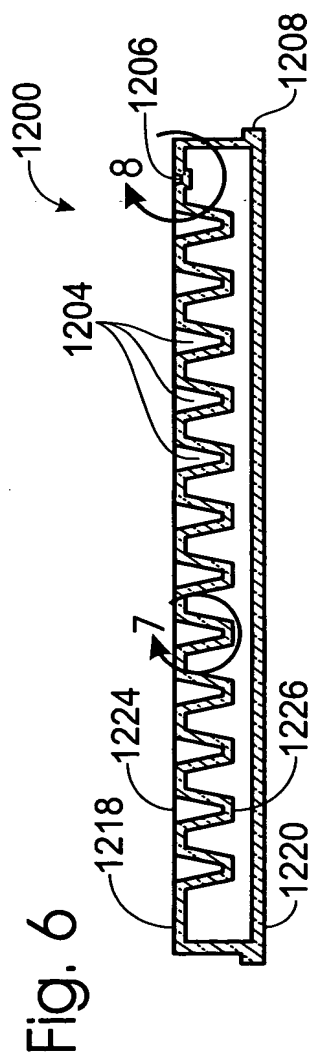
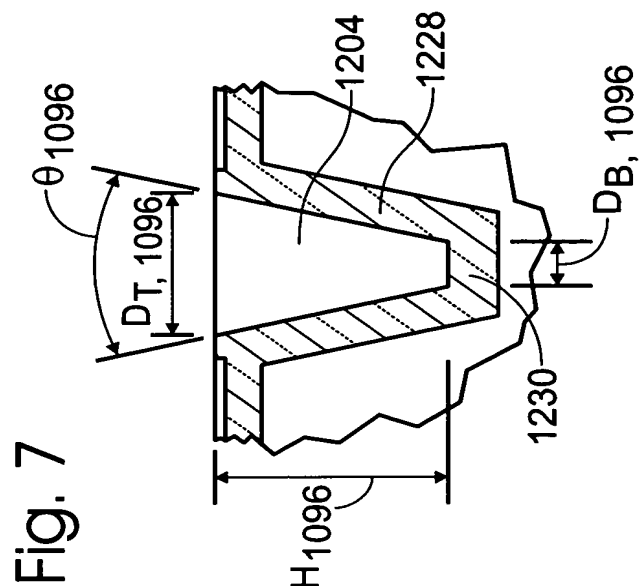
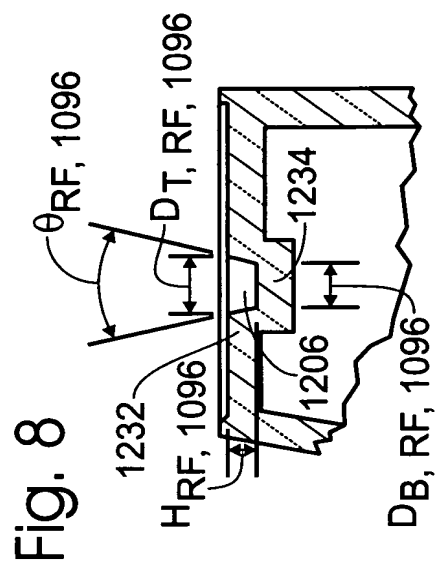
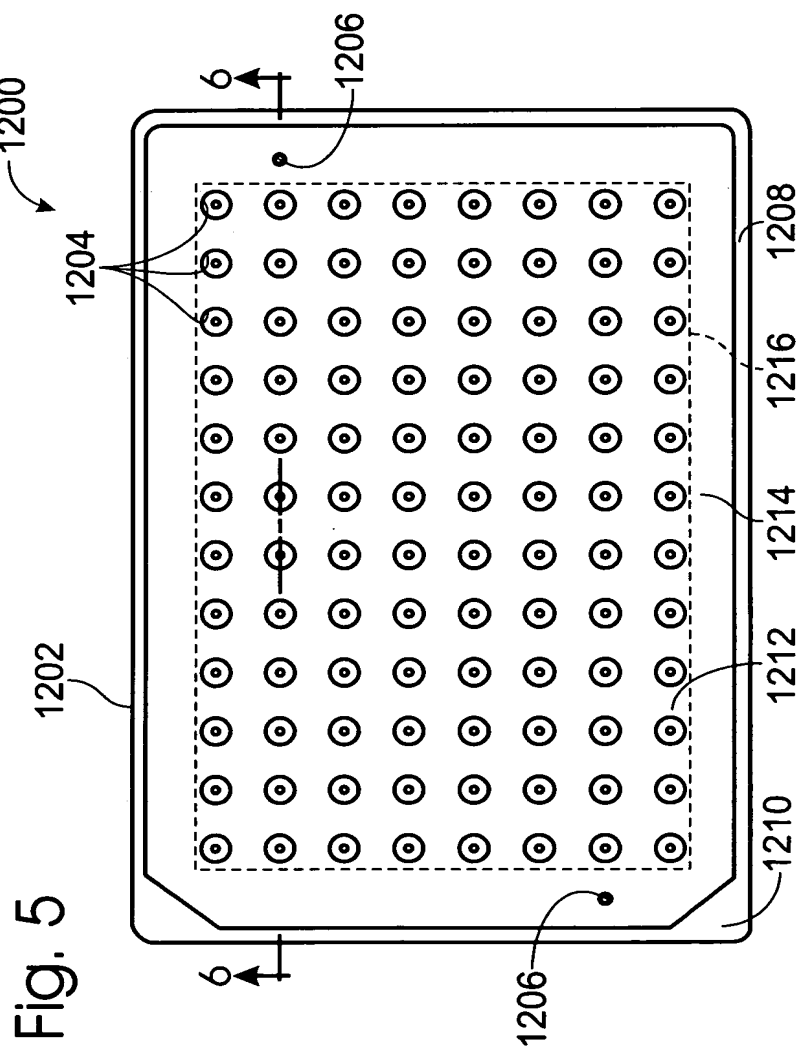


Fig. 4





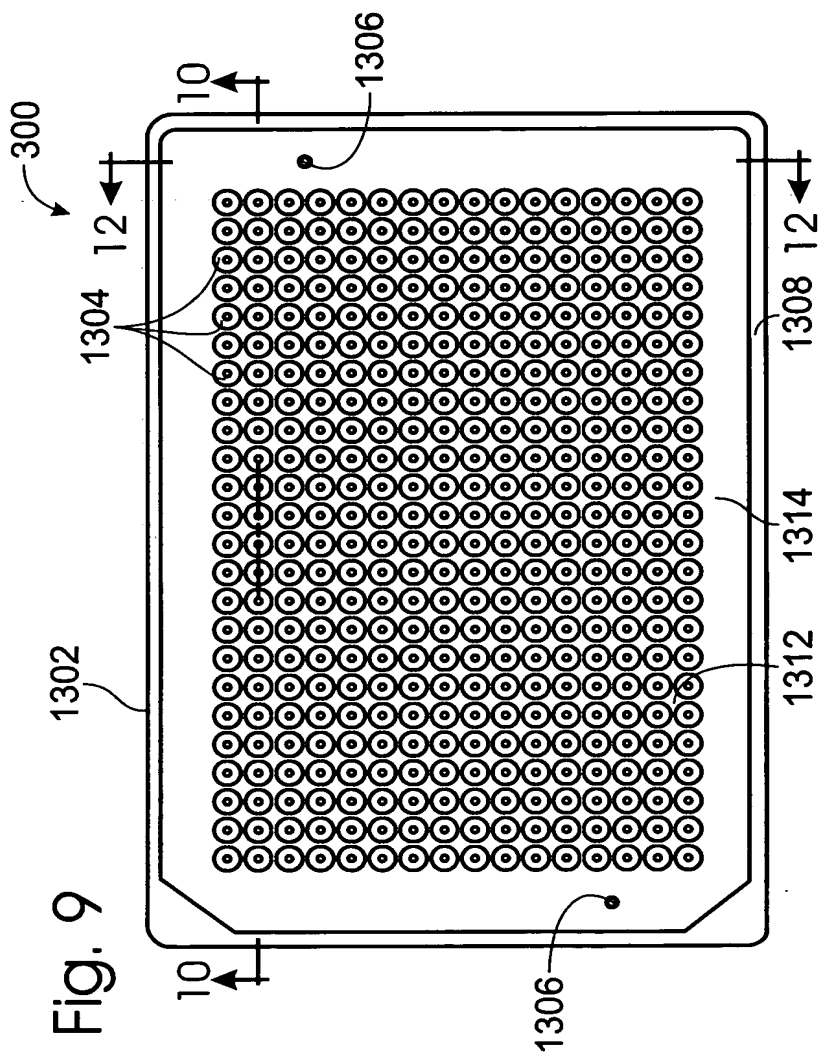


Fig. 12

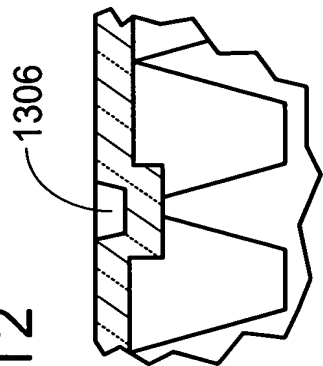


Fig. 11

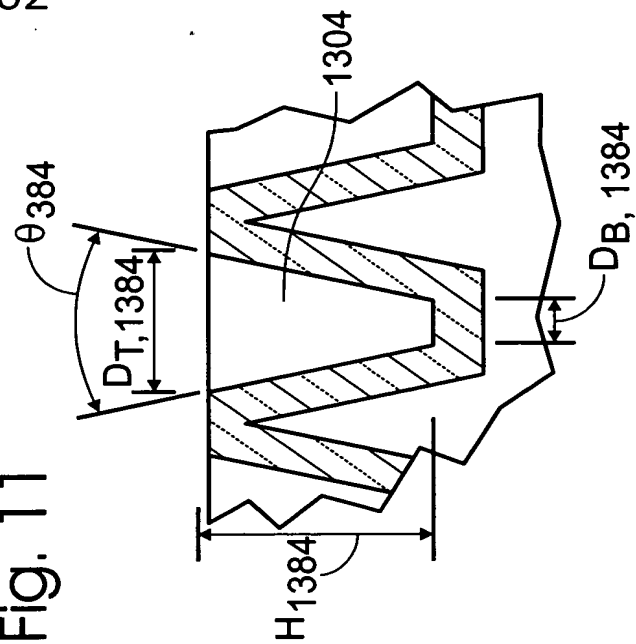


Fig. 10

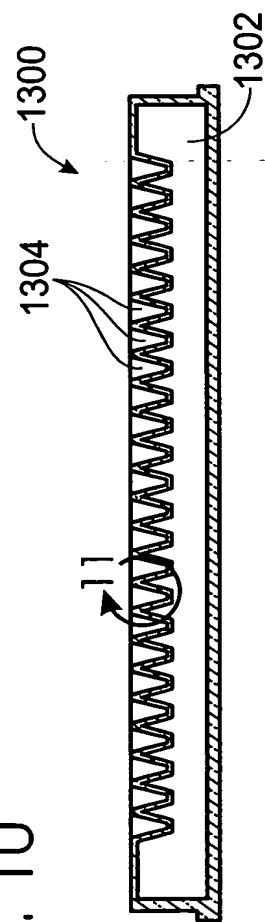


Fig. 13

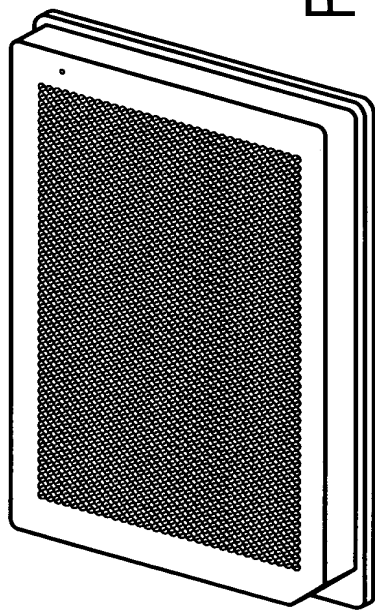


Fig. 15

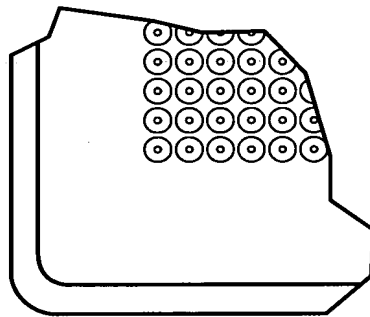


Fig. 17

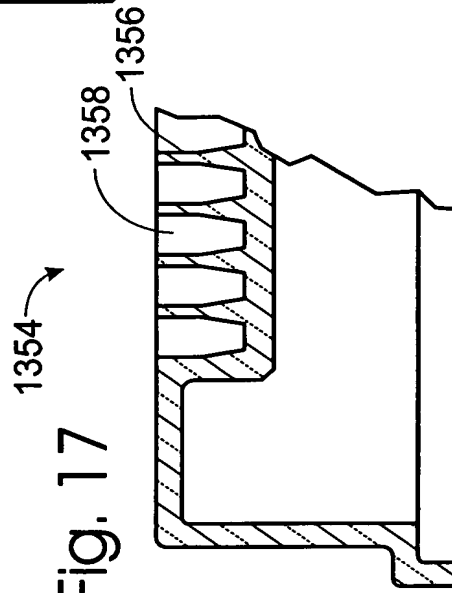


Fig. 14

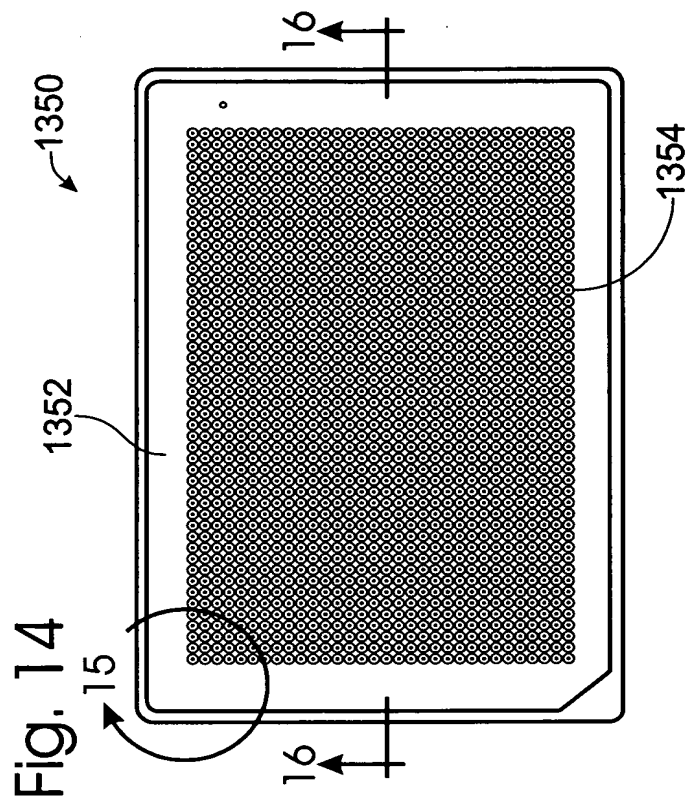
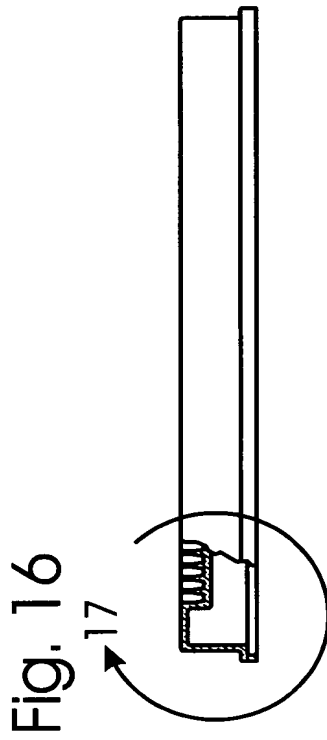


Fig. 16



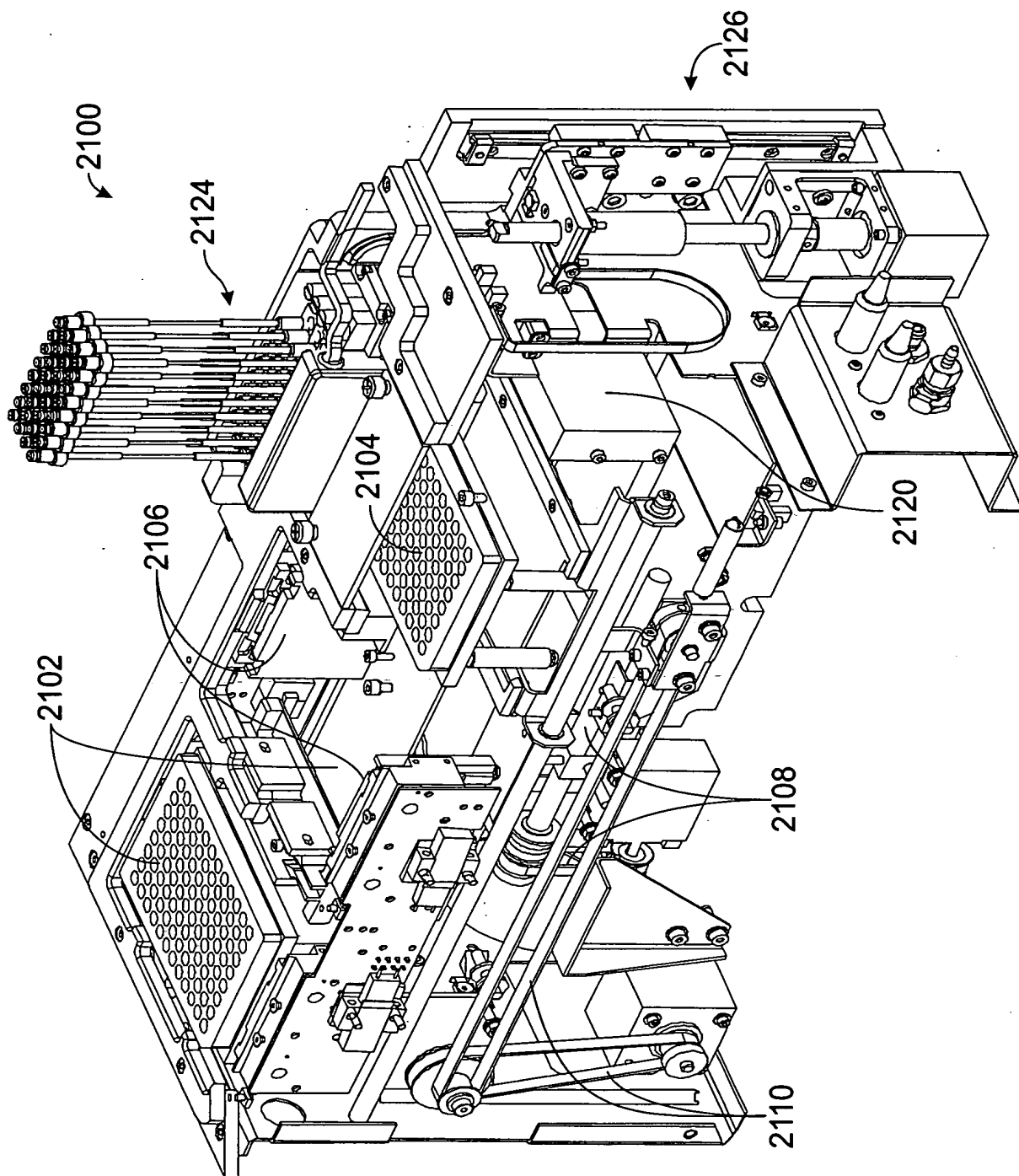


Fig. 18

Fig. 20

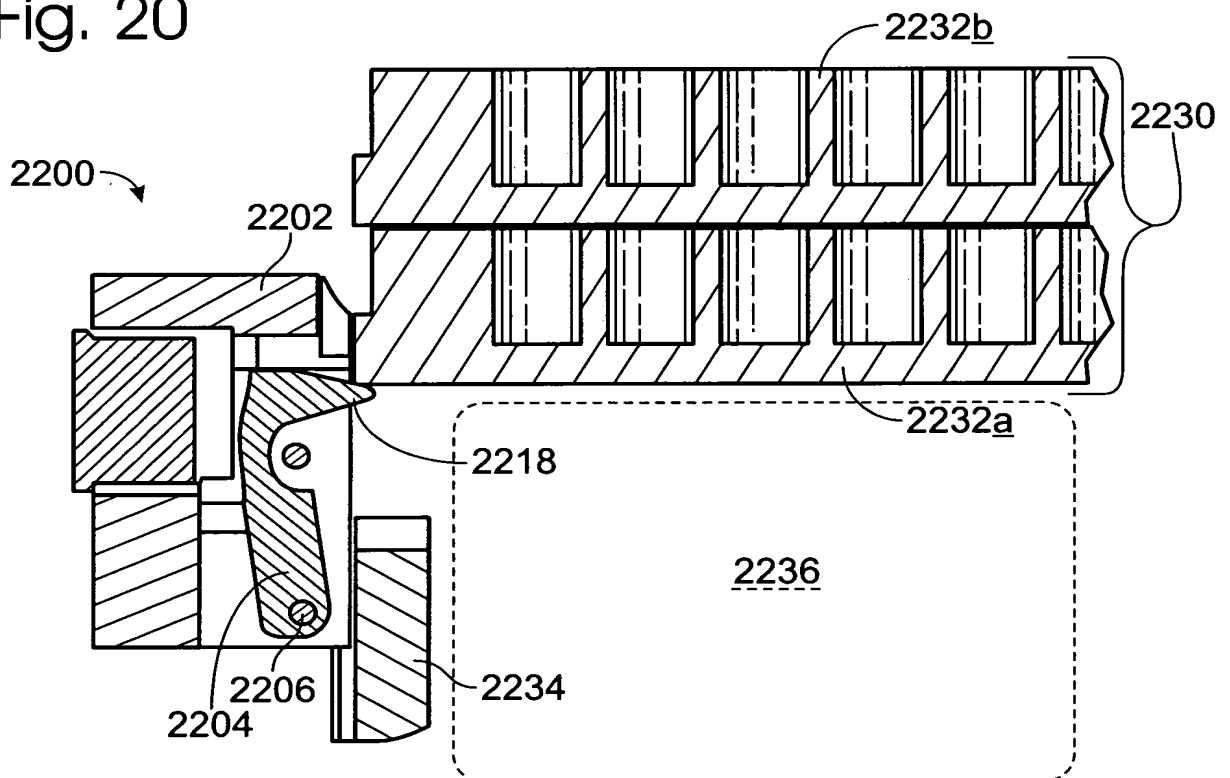




Fig. 21 (INPUT CYCLE)

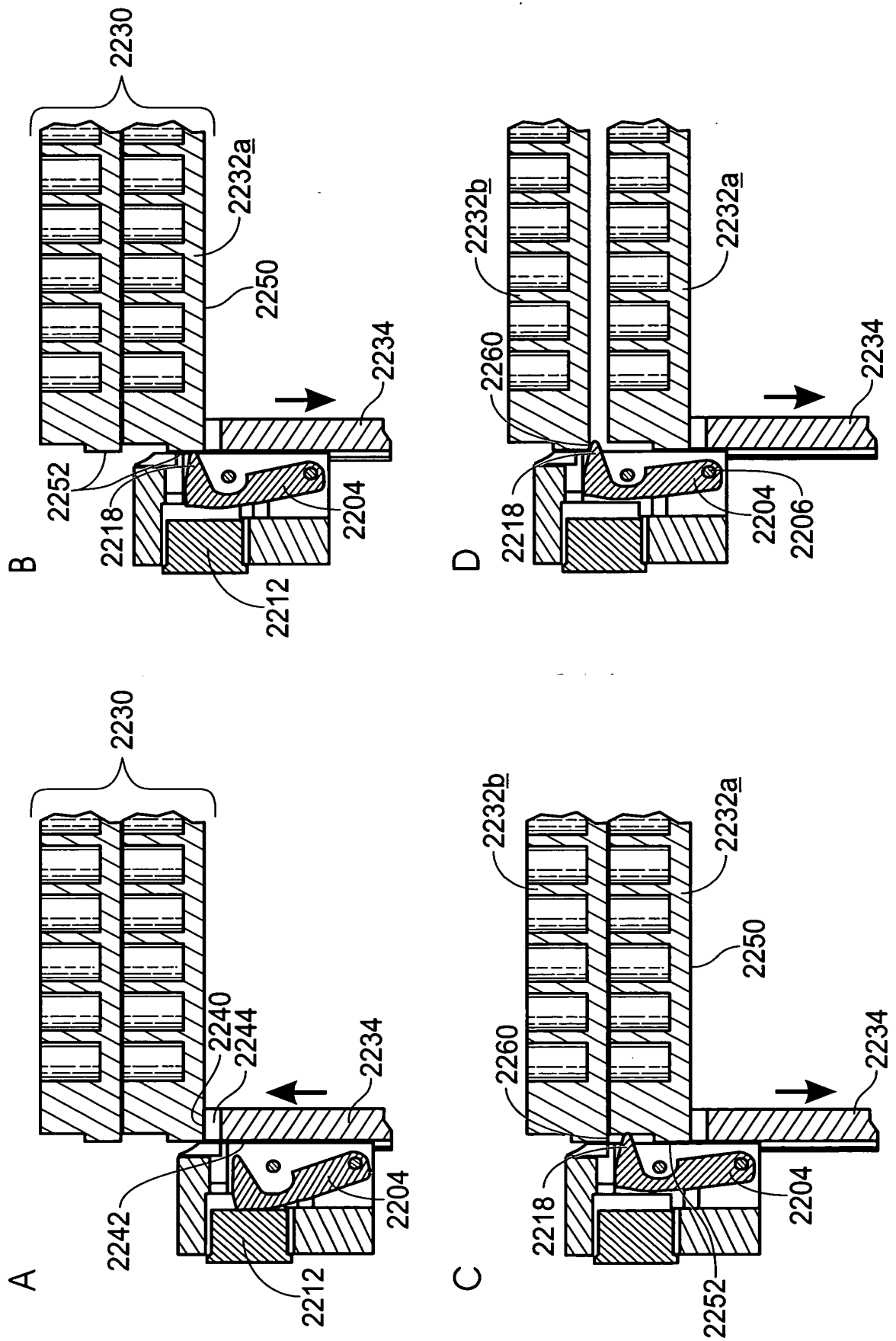


Fig. 22 (OUTPUT CYCLE)

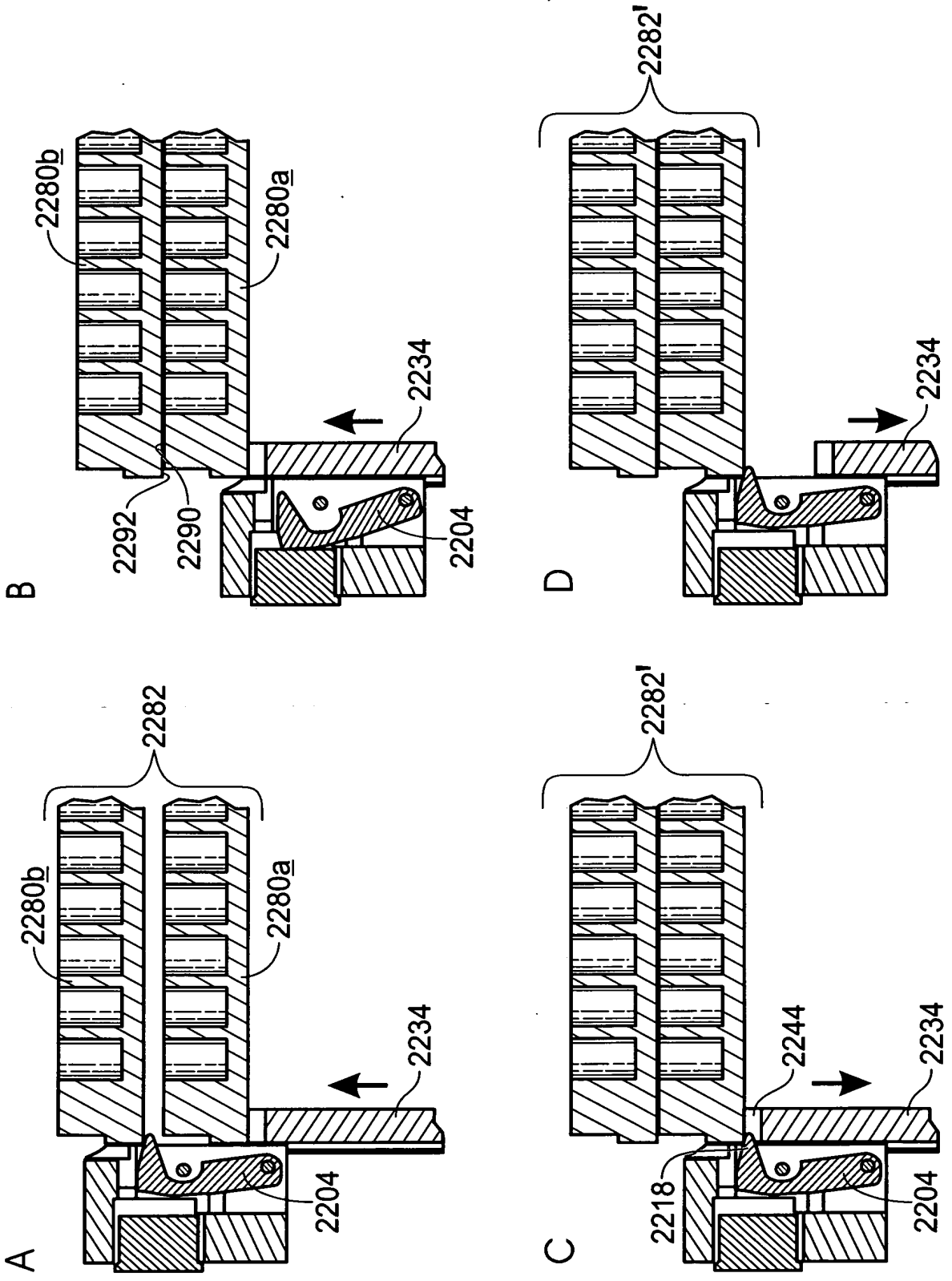


Fig. 23

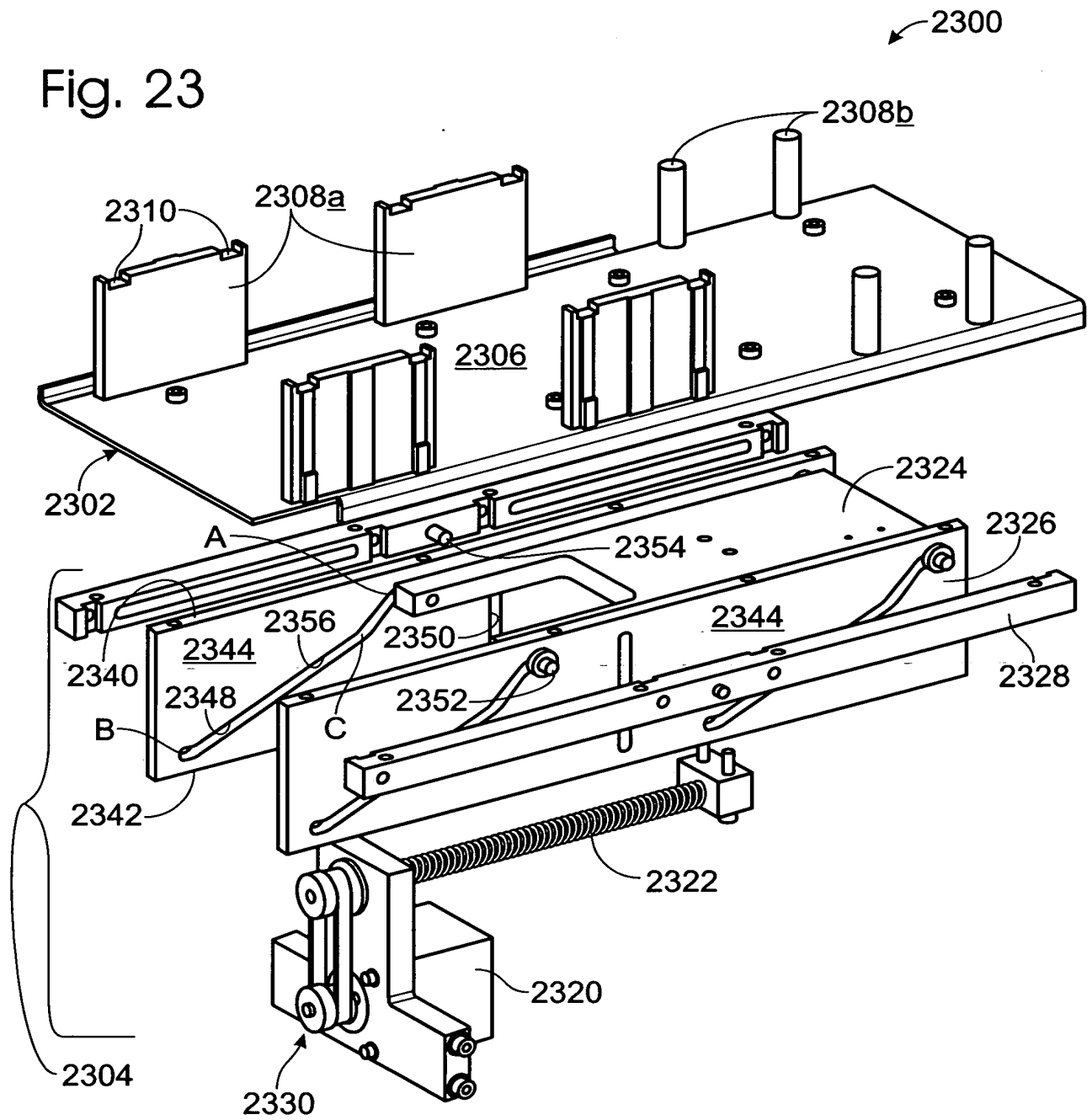


FIG. 24

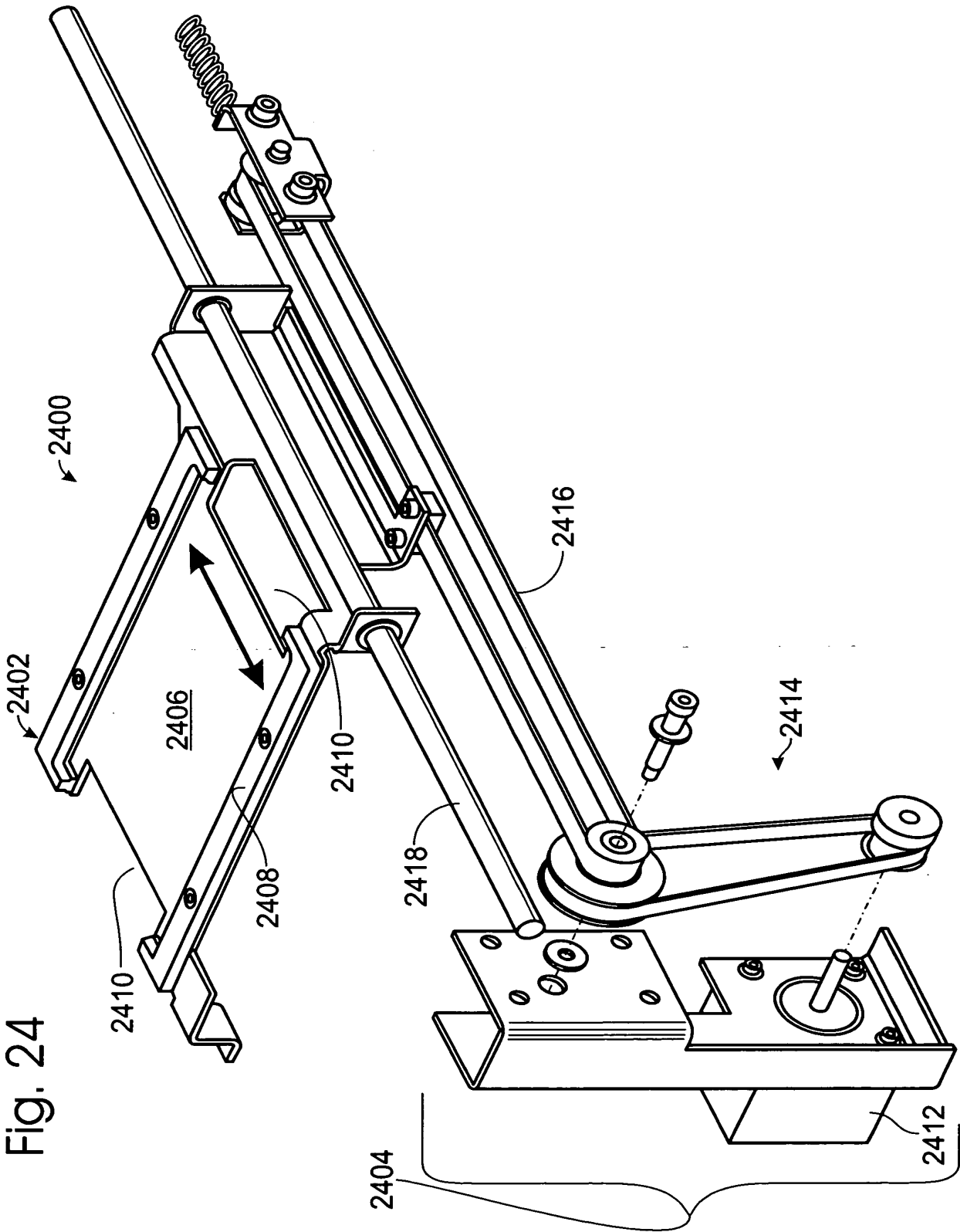


Fig. 25

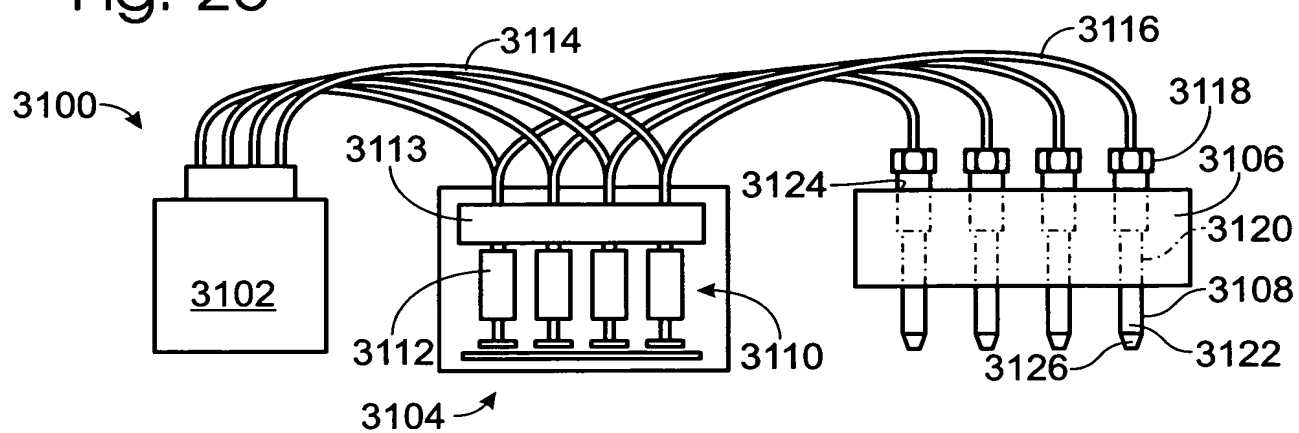


Fig. 26

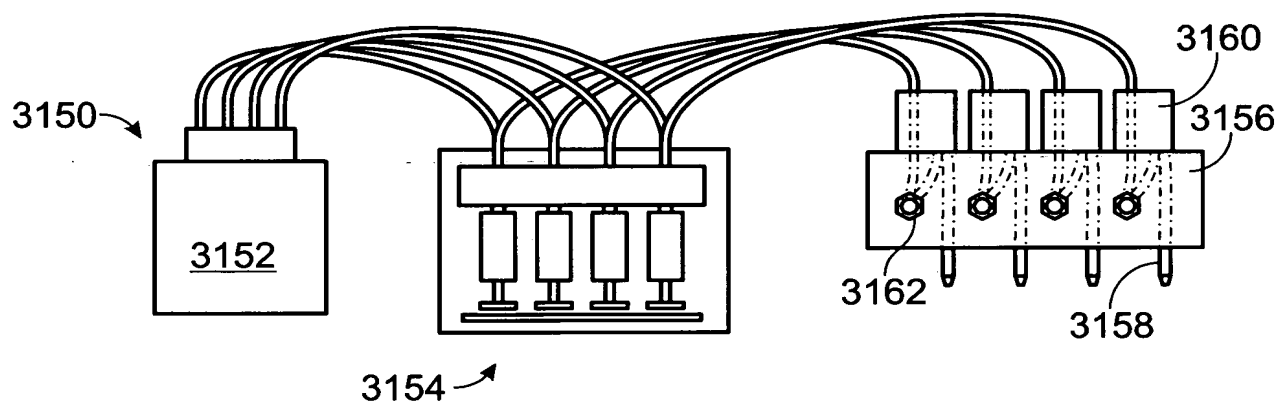


Fig. 27

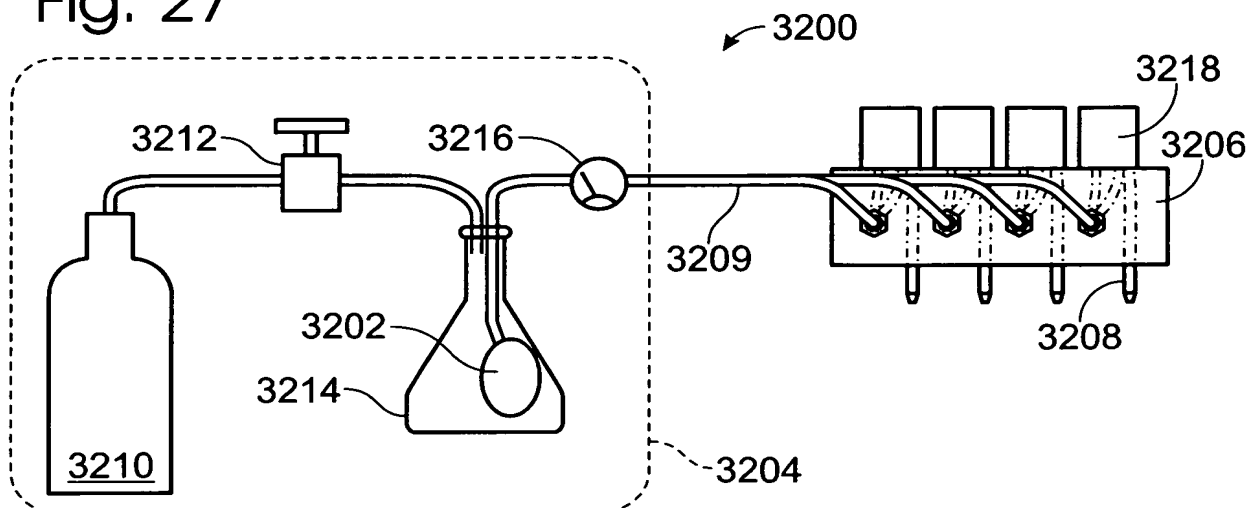


Fig. 28

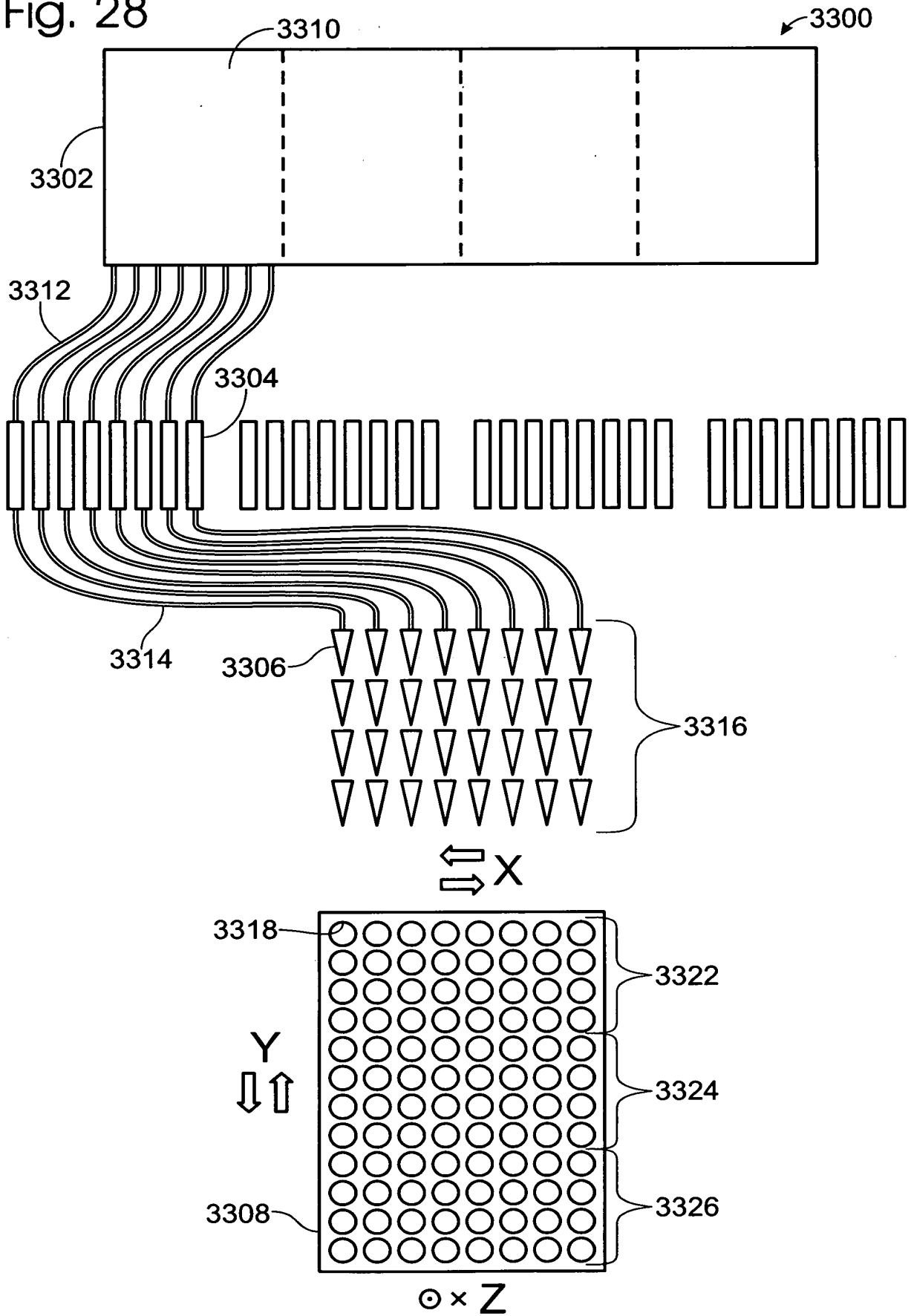


Fig. 29

3402

3404

3420

3400

3412b

X

Y

Z

3406

3410

3416

3412a

3414

3410

Fig. 30

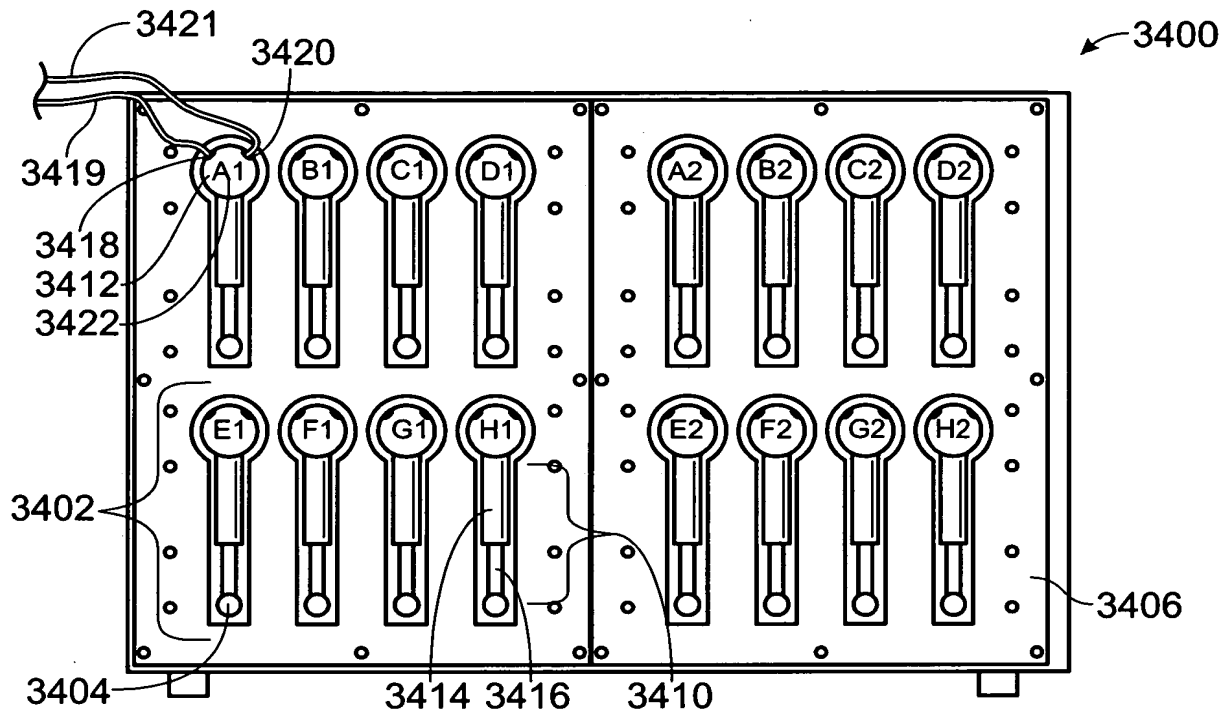


Fig. 31

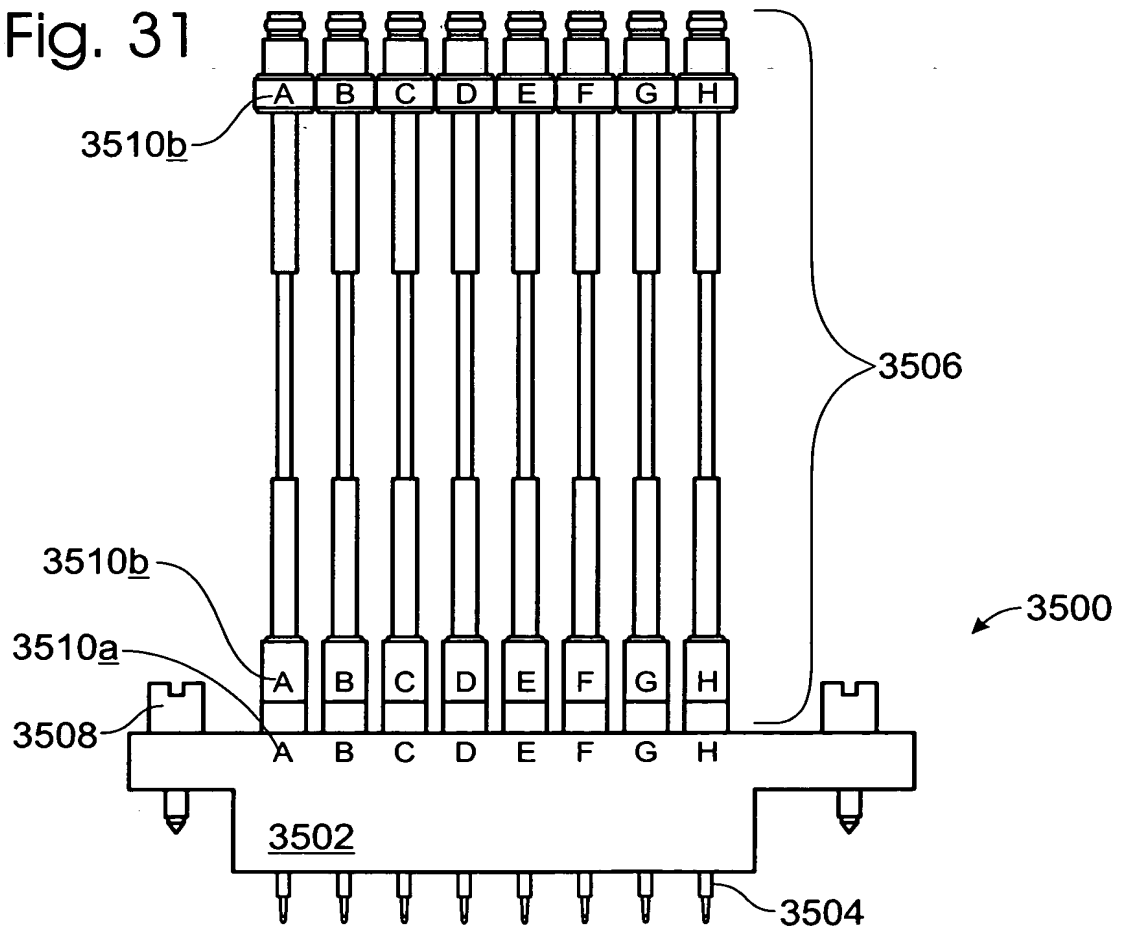




Fig. 32

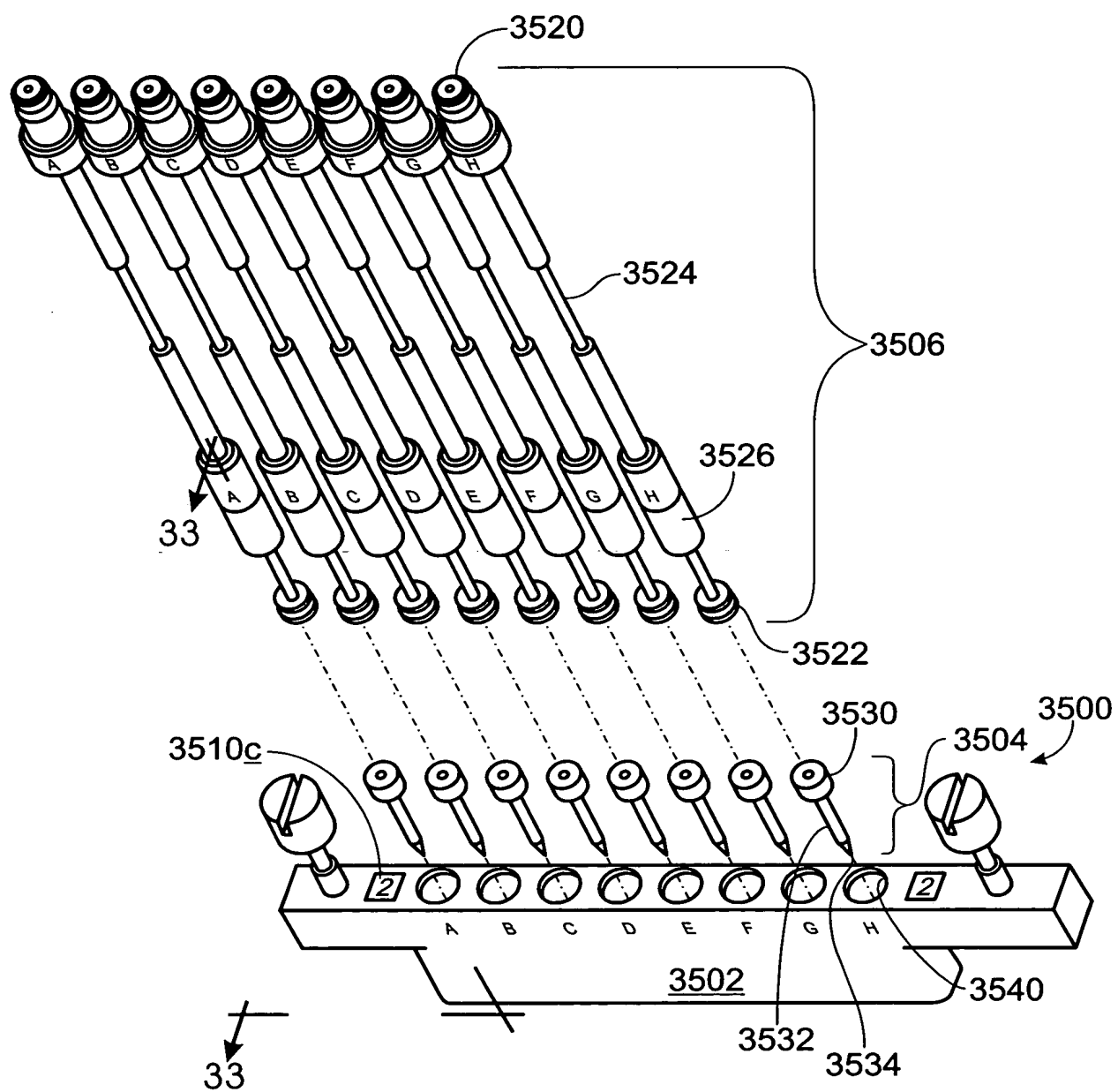


Fig. 33

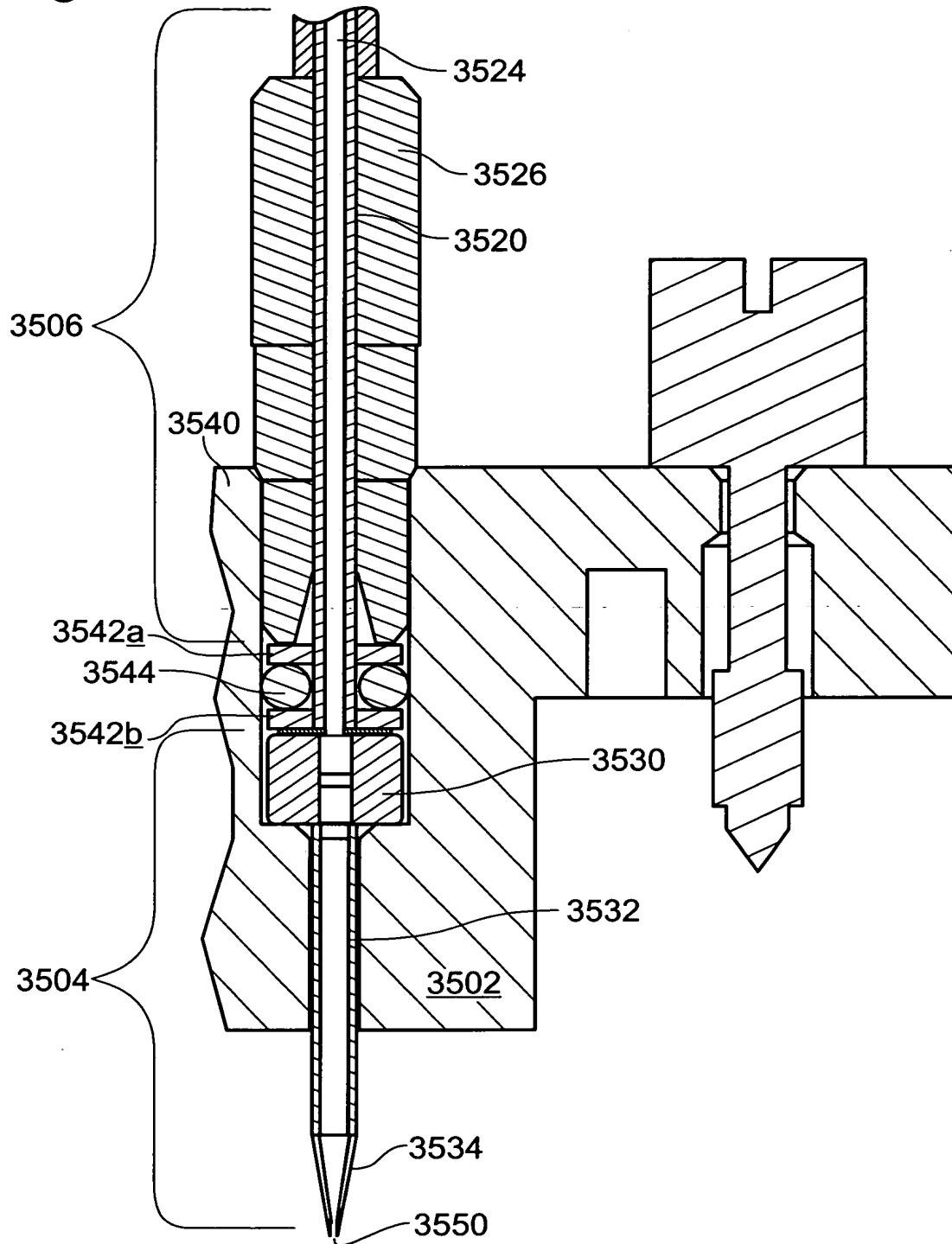


Fig. 34

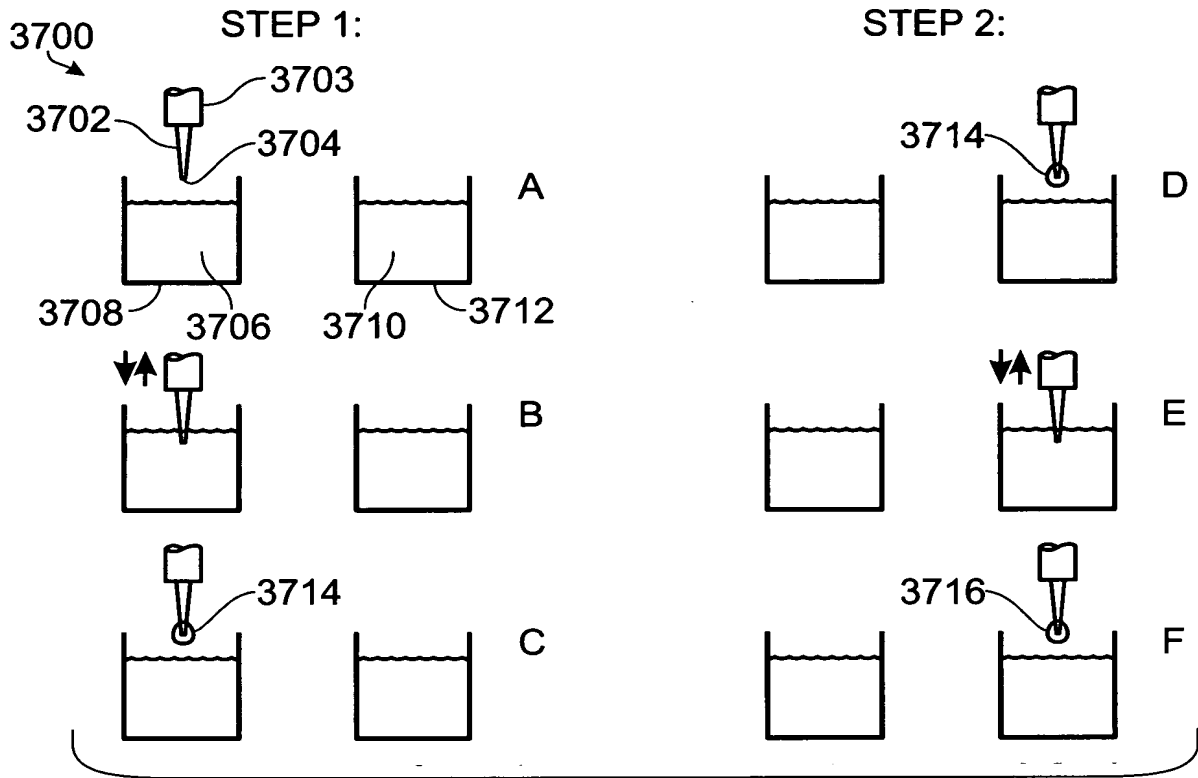


Fig. 35

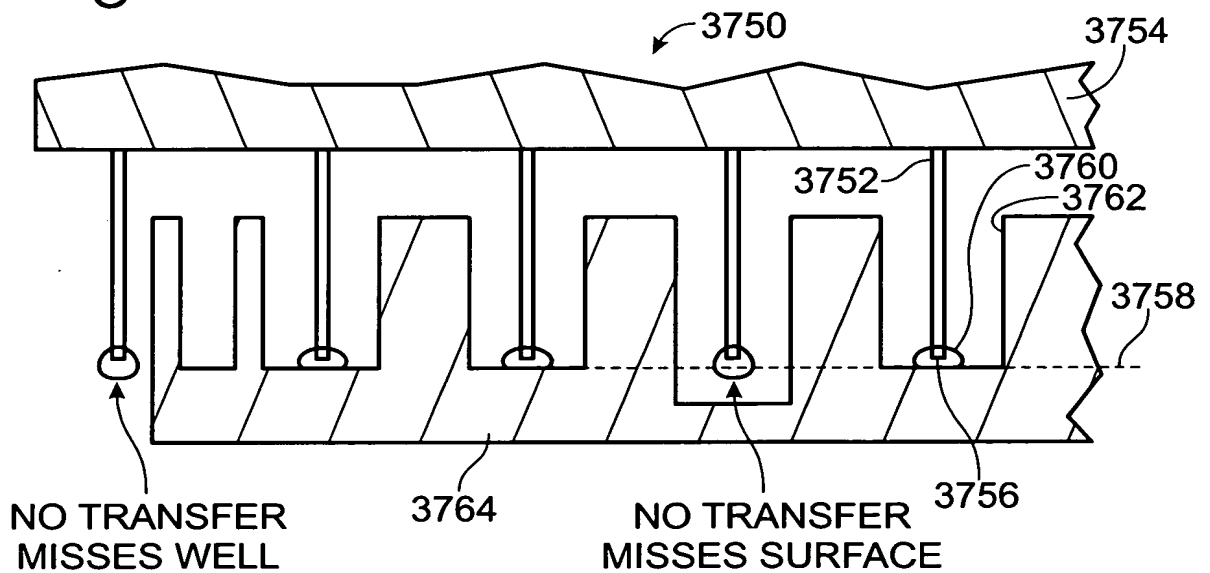


Fig. 36

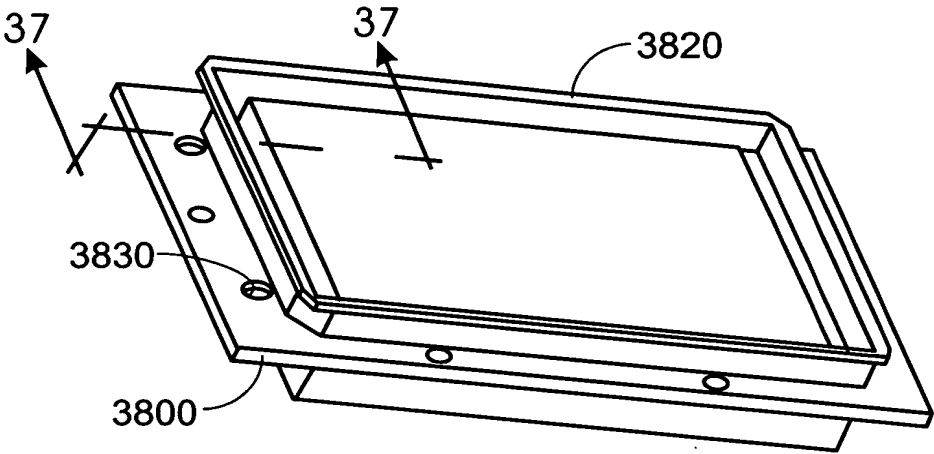


Fig. 37

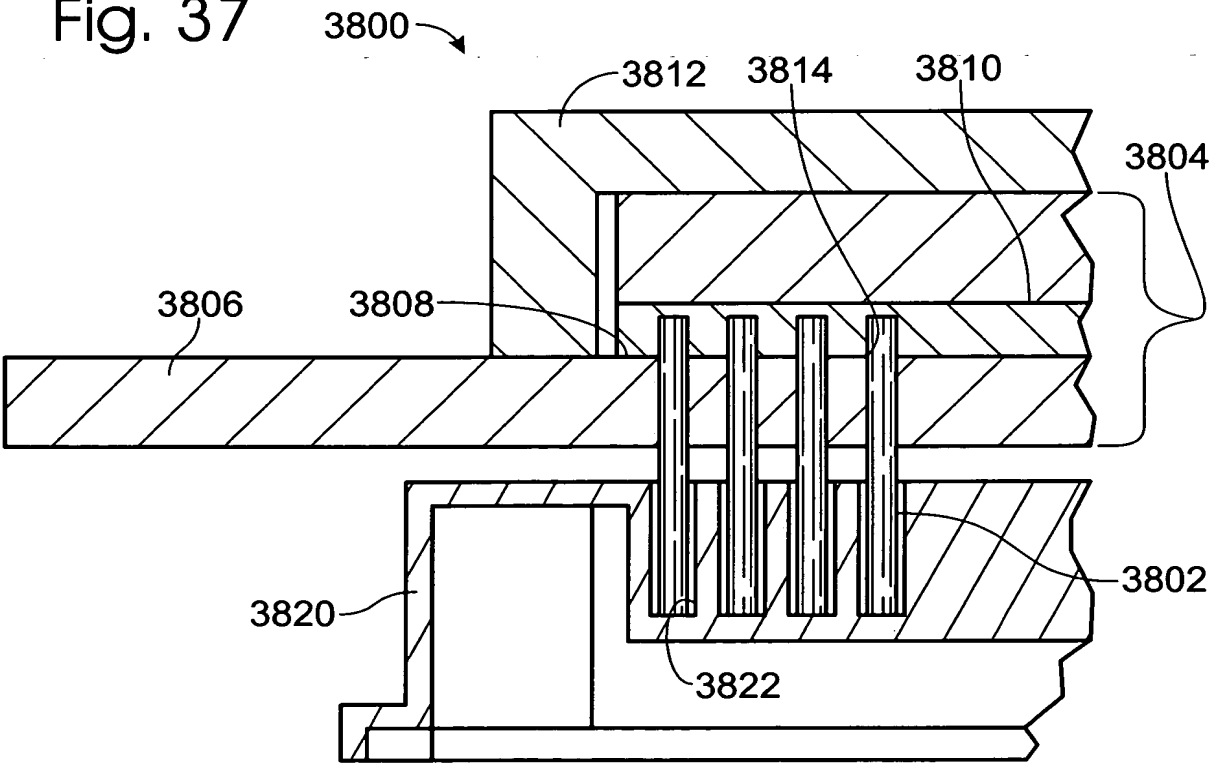


Fig. 38

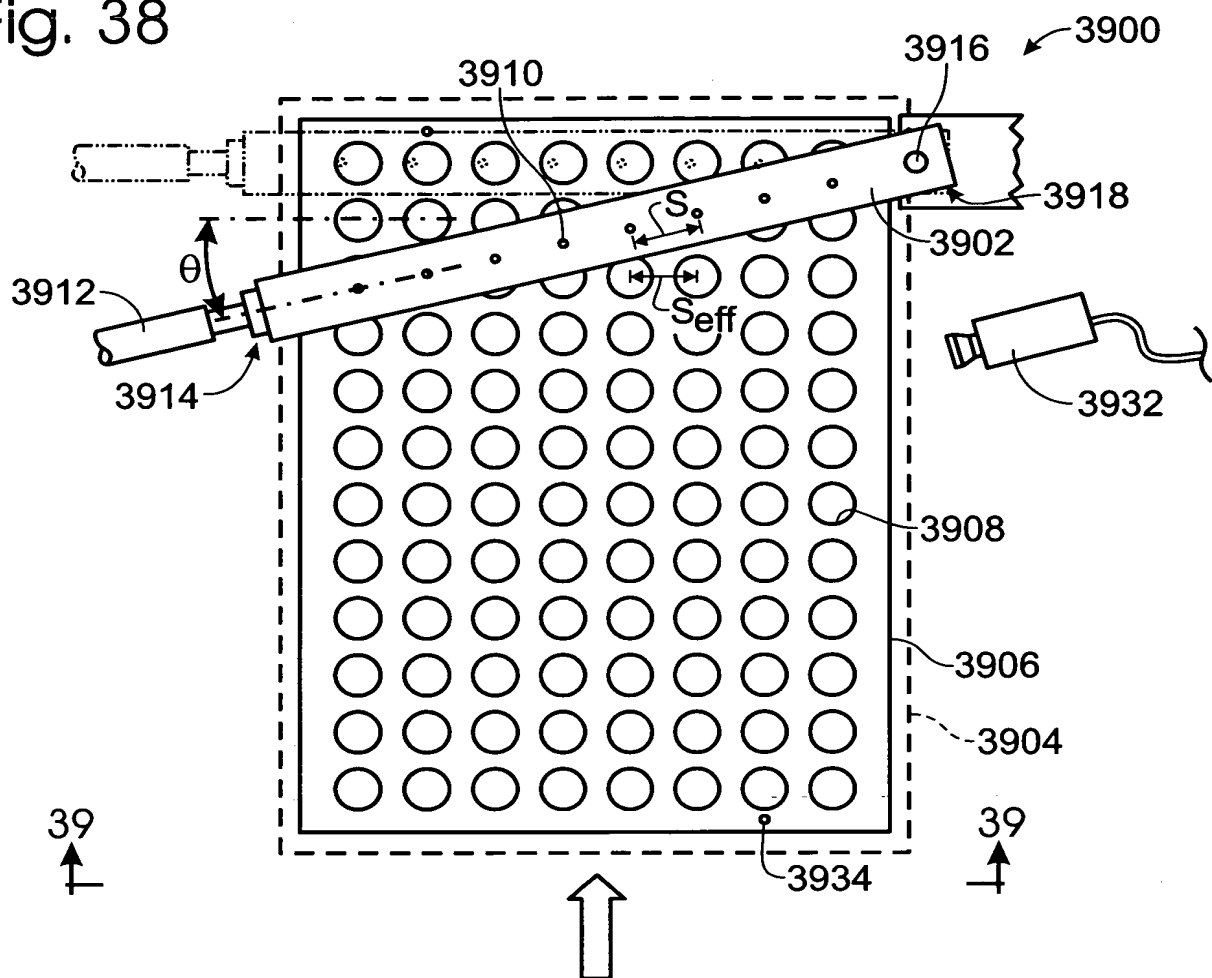


Fig. 39

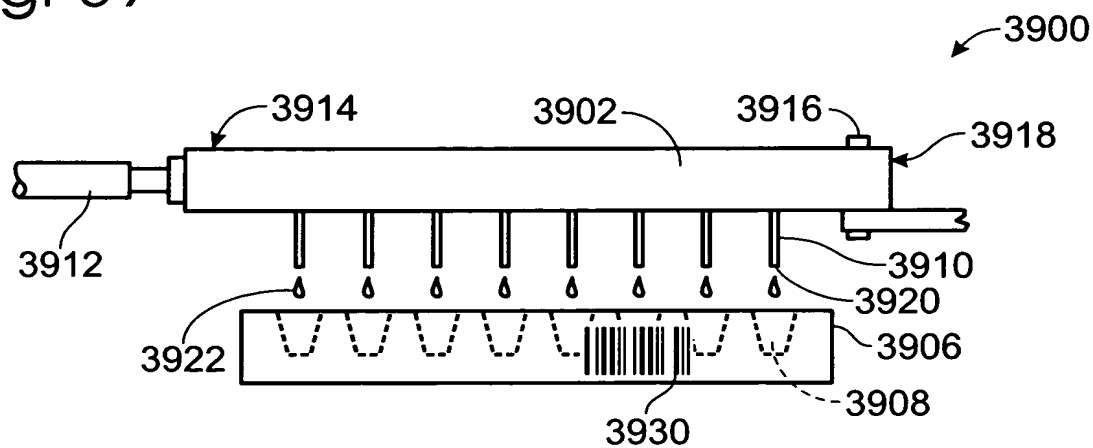


Fig. 40

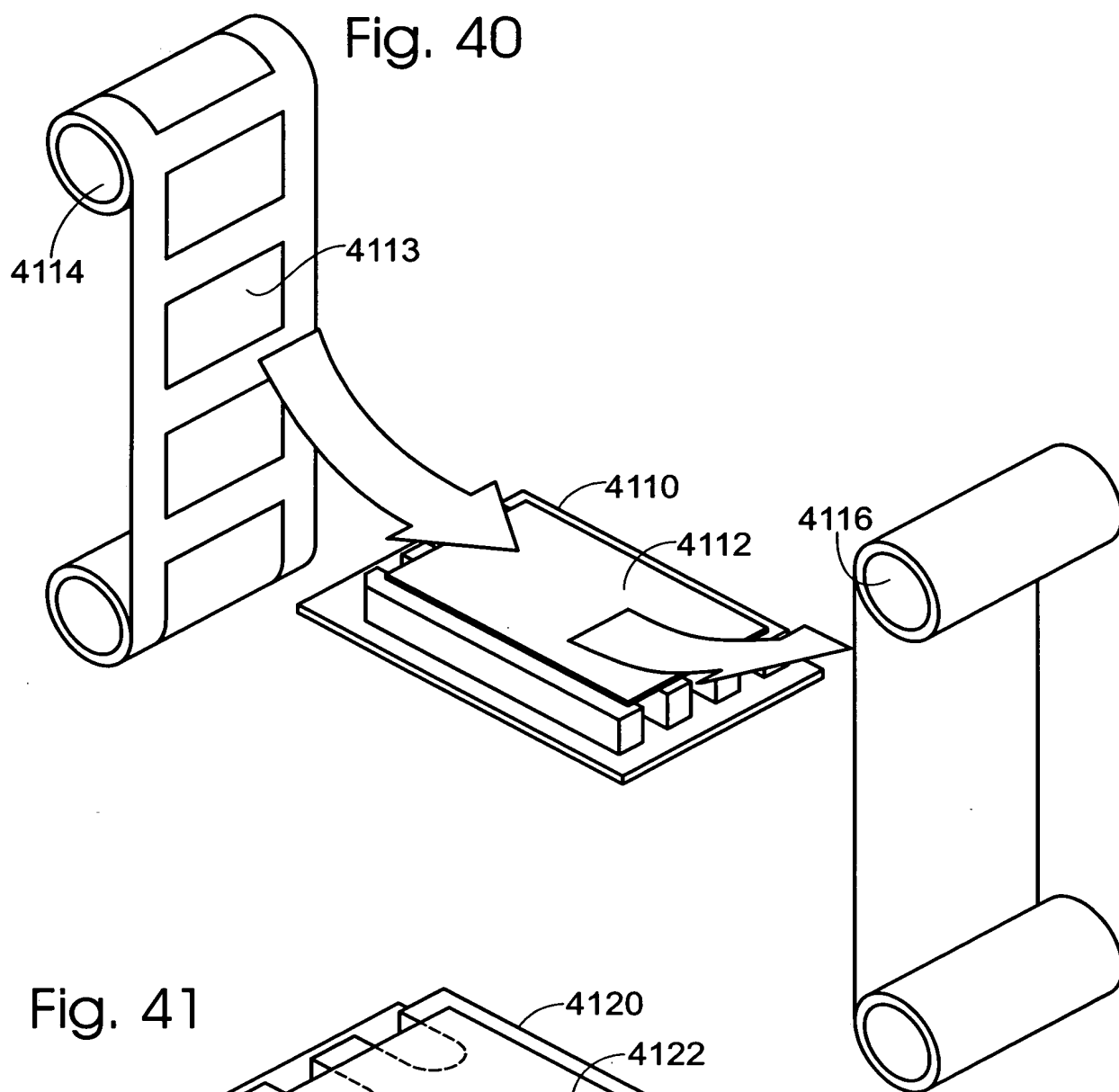


Fig. 41

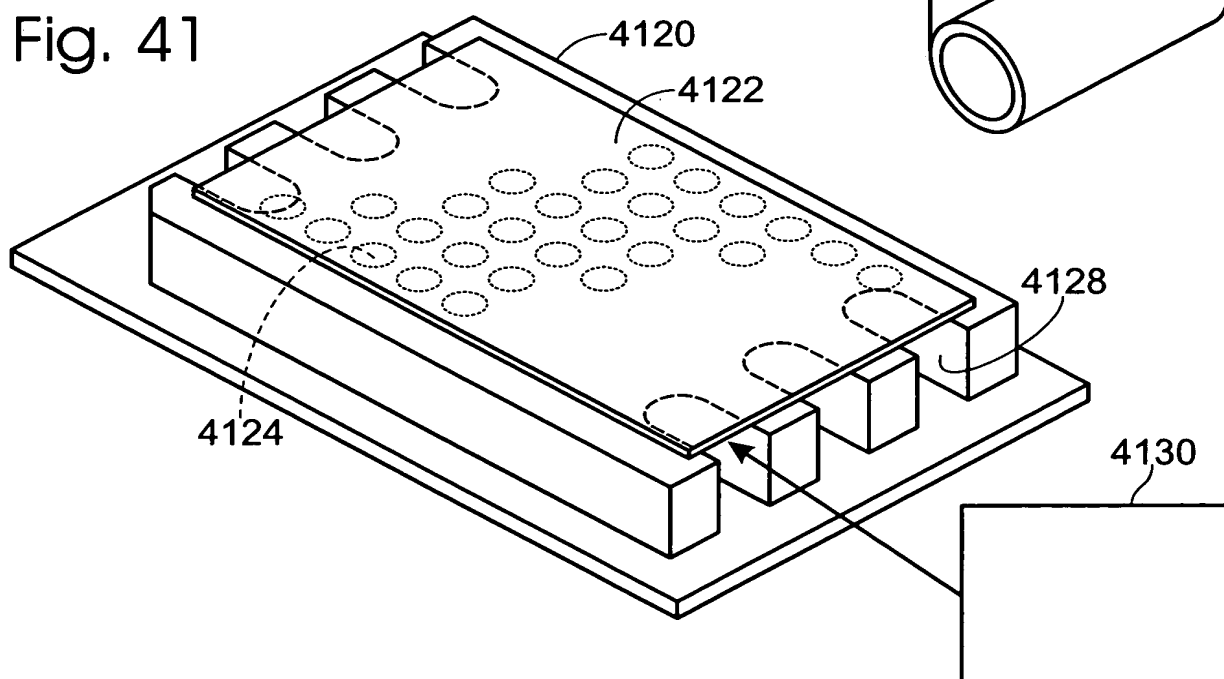


Fig. 42

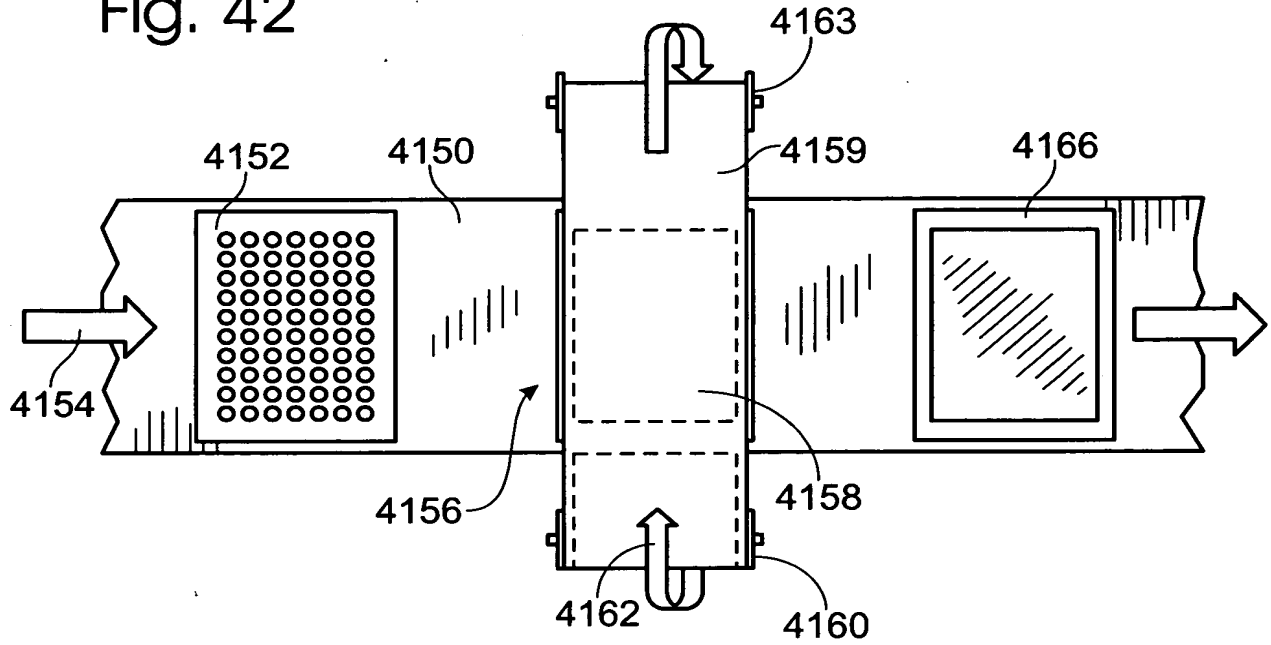


Fig. 43

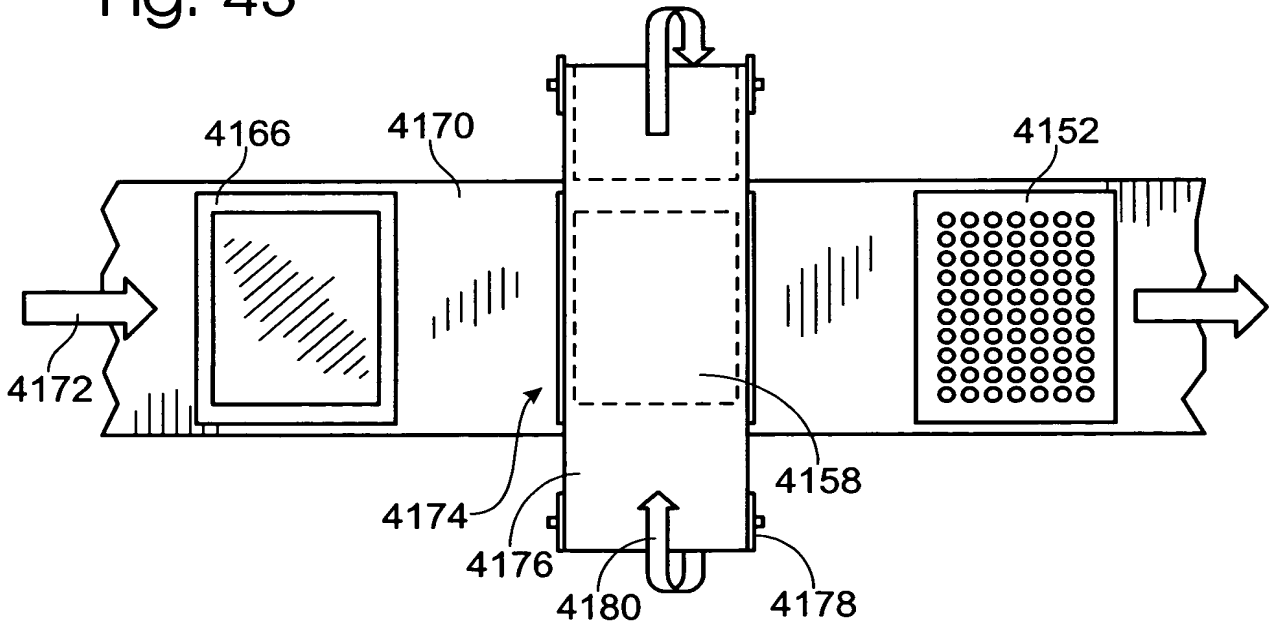


Fig. 44

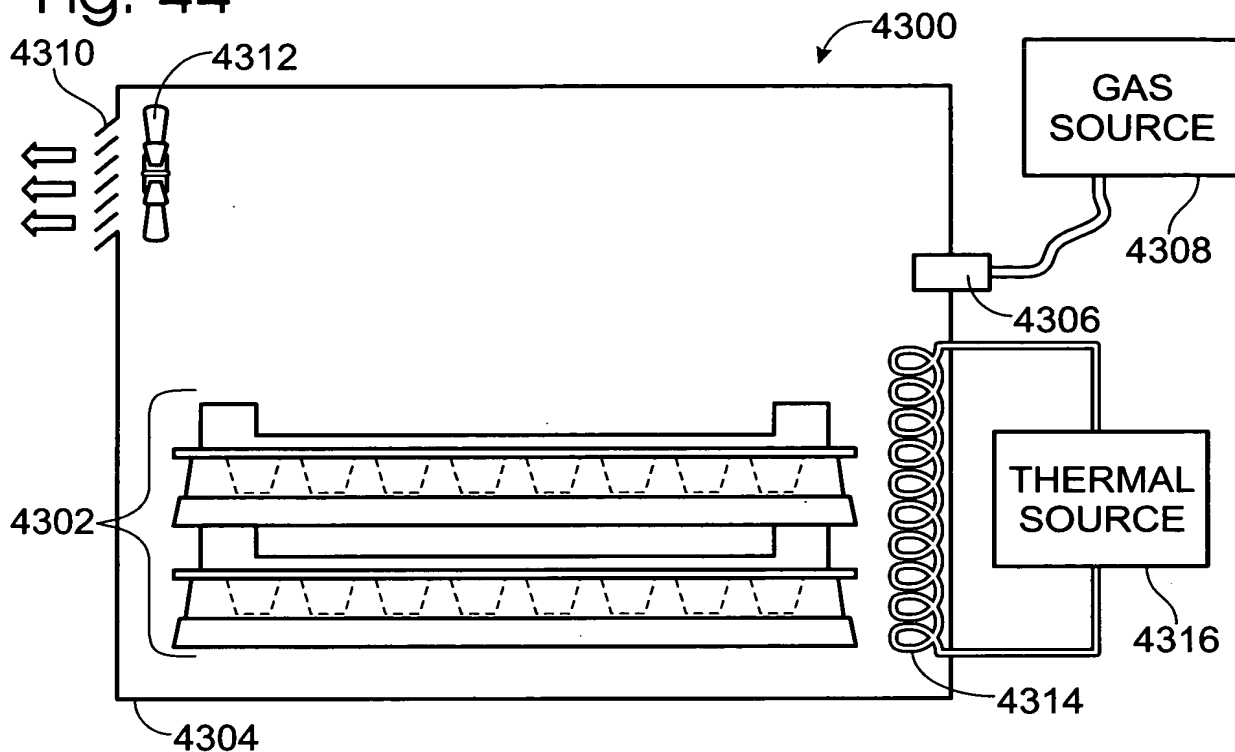


Fig. 45

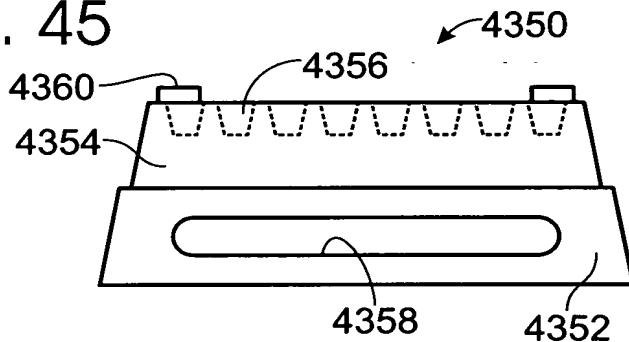


Fig. 46

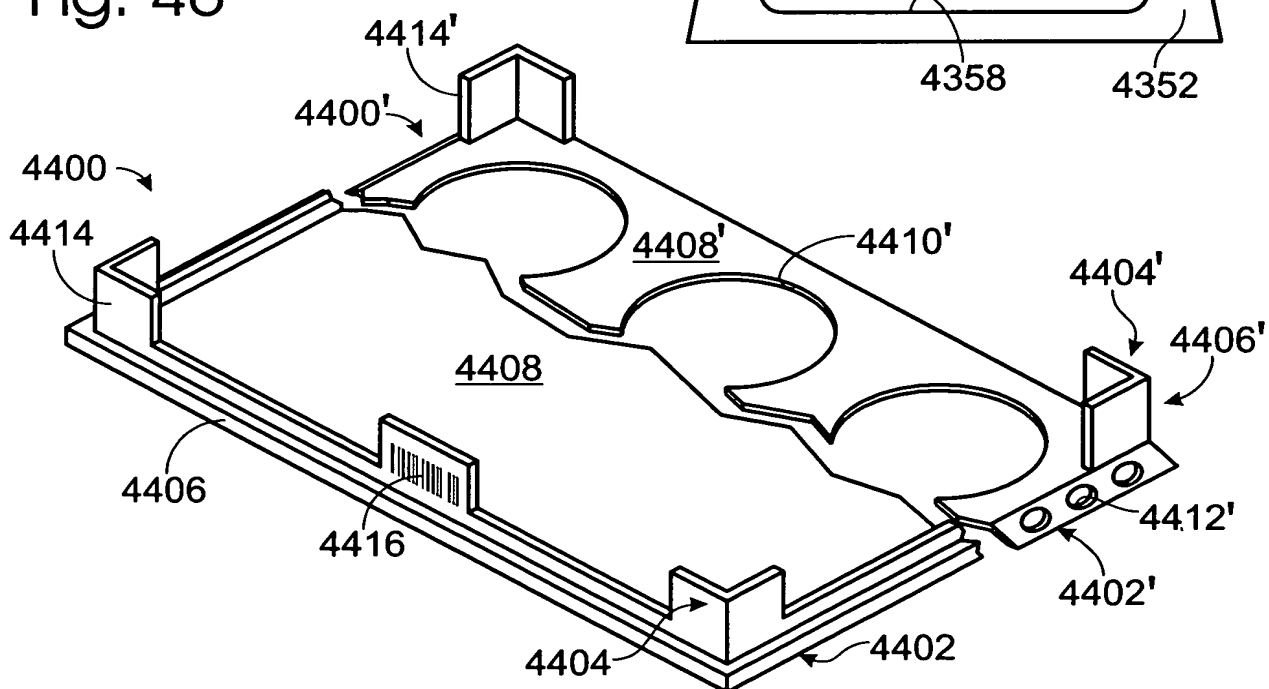




Fig. 47

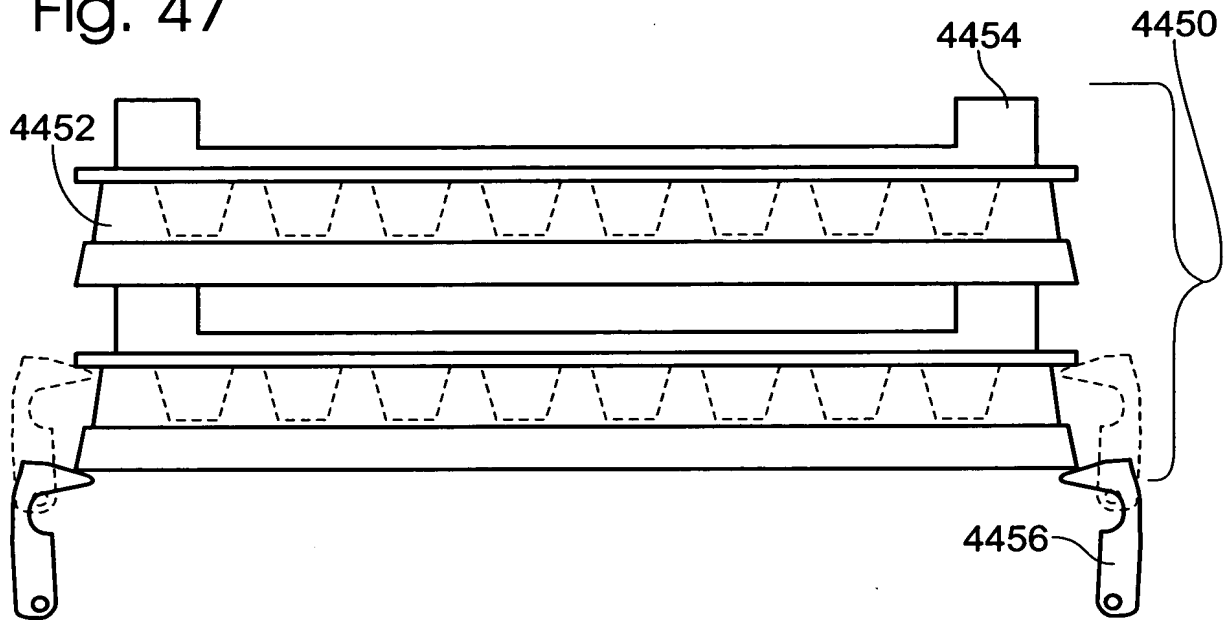
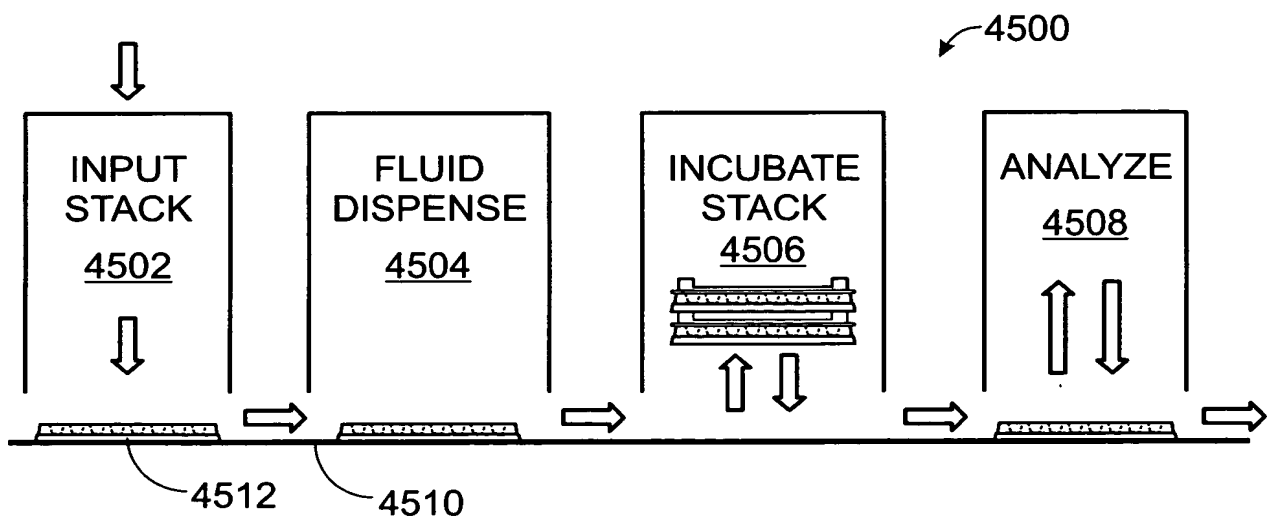


Fig. 48



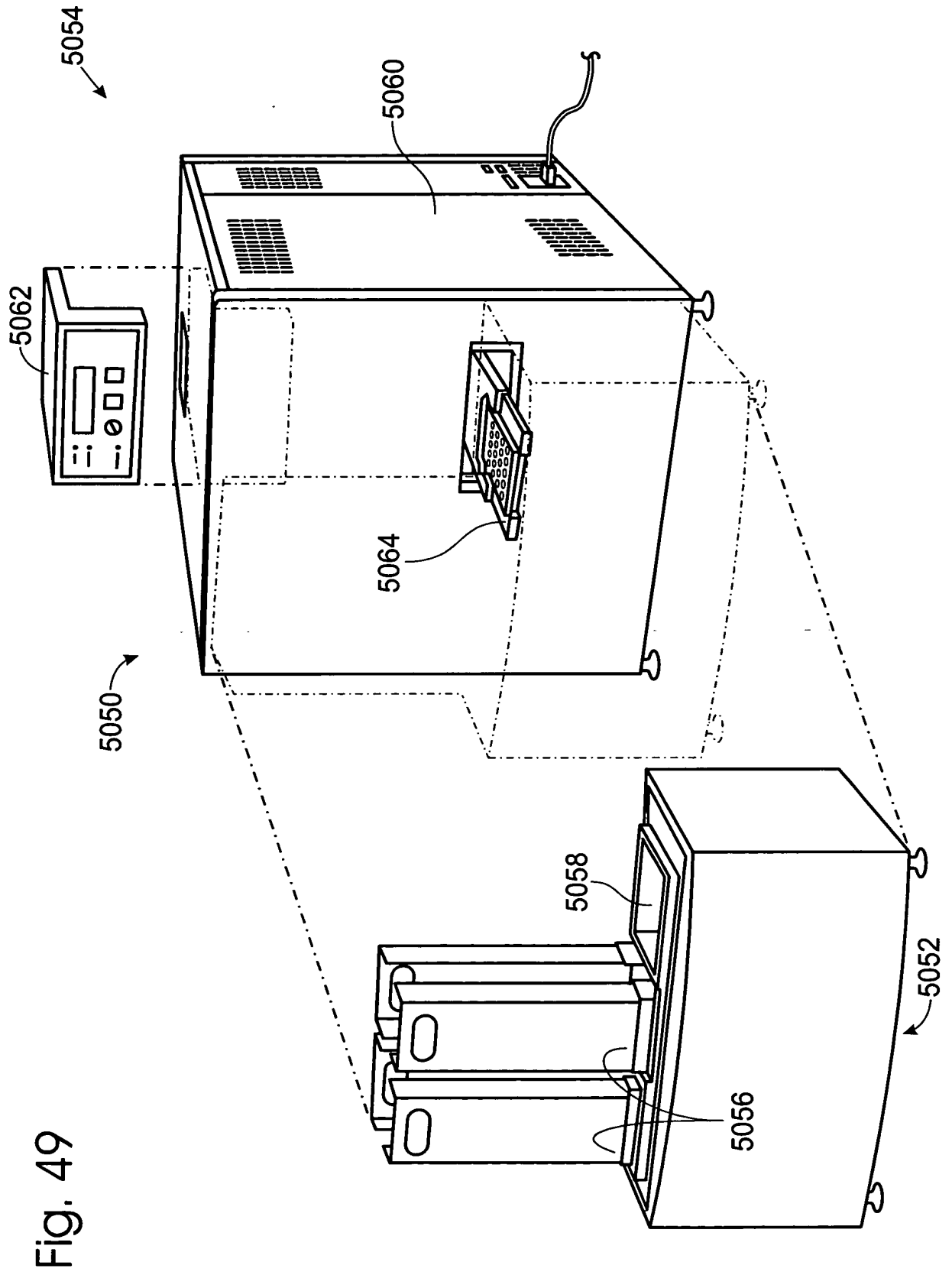


FIG. 49

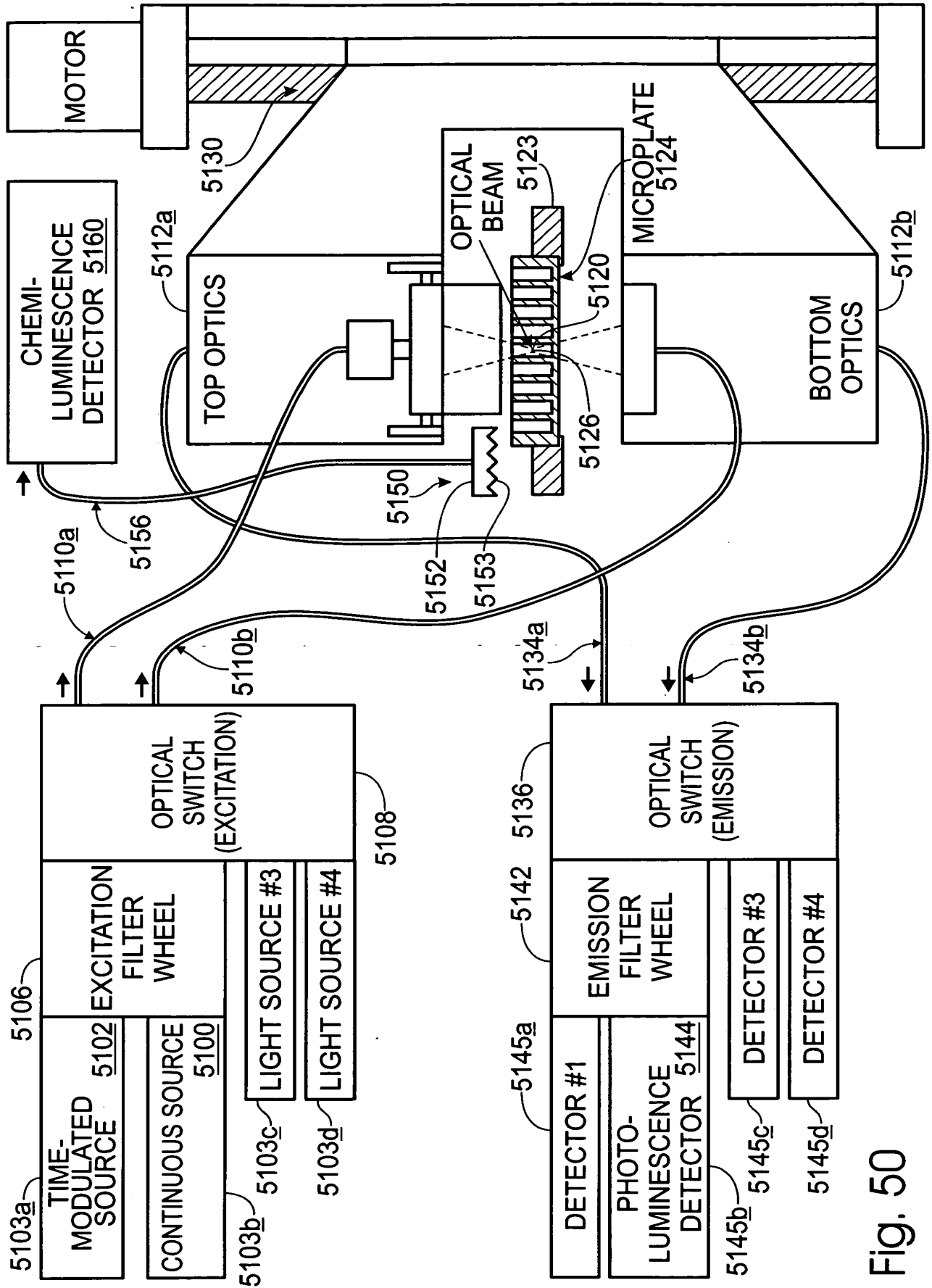


Fig. 50

Fig. 51

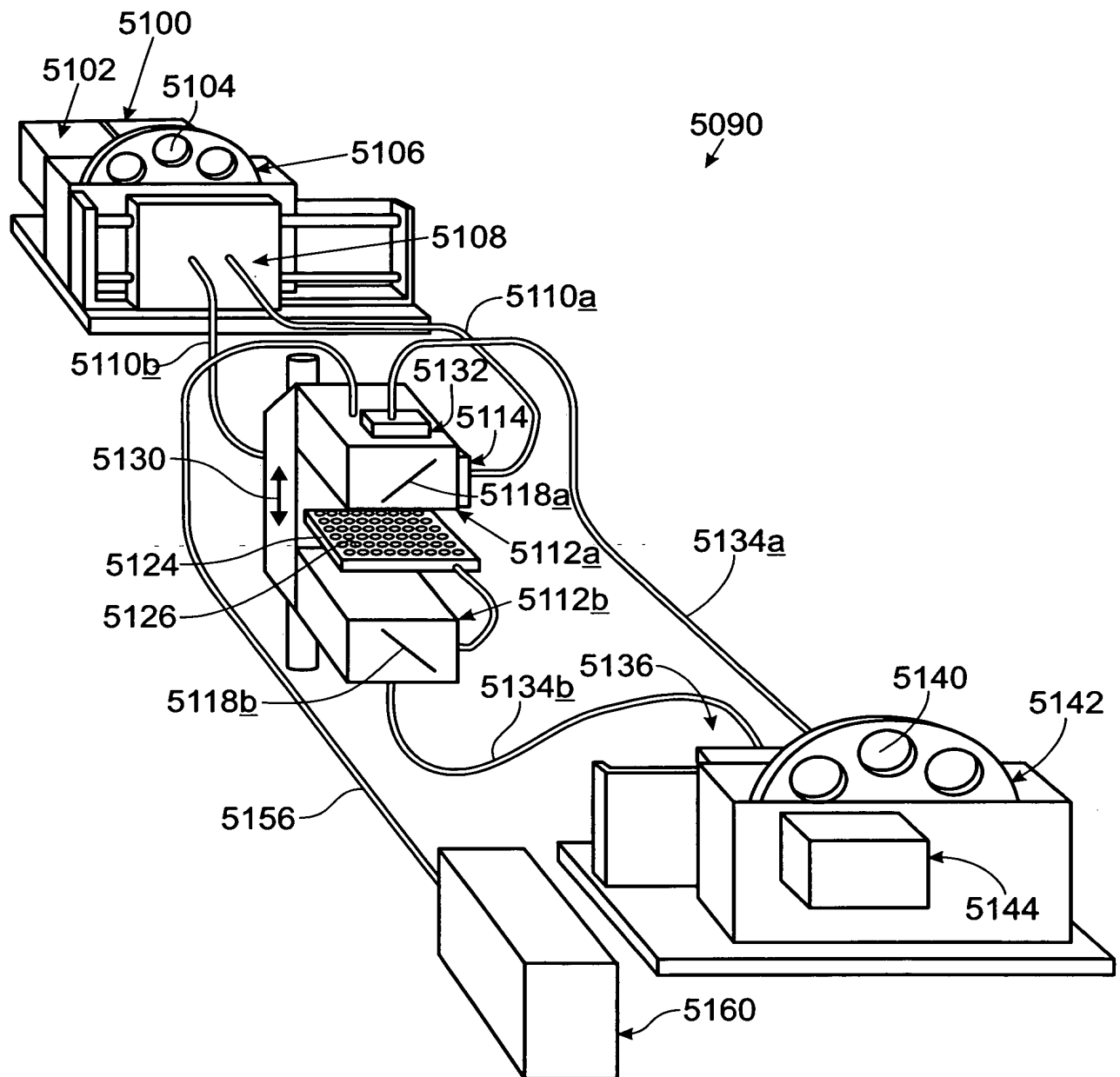


Fig. 52

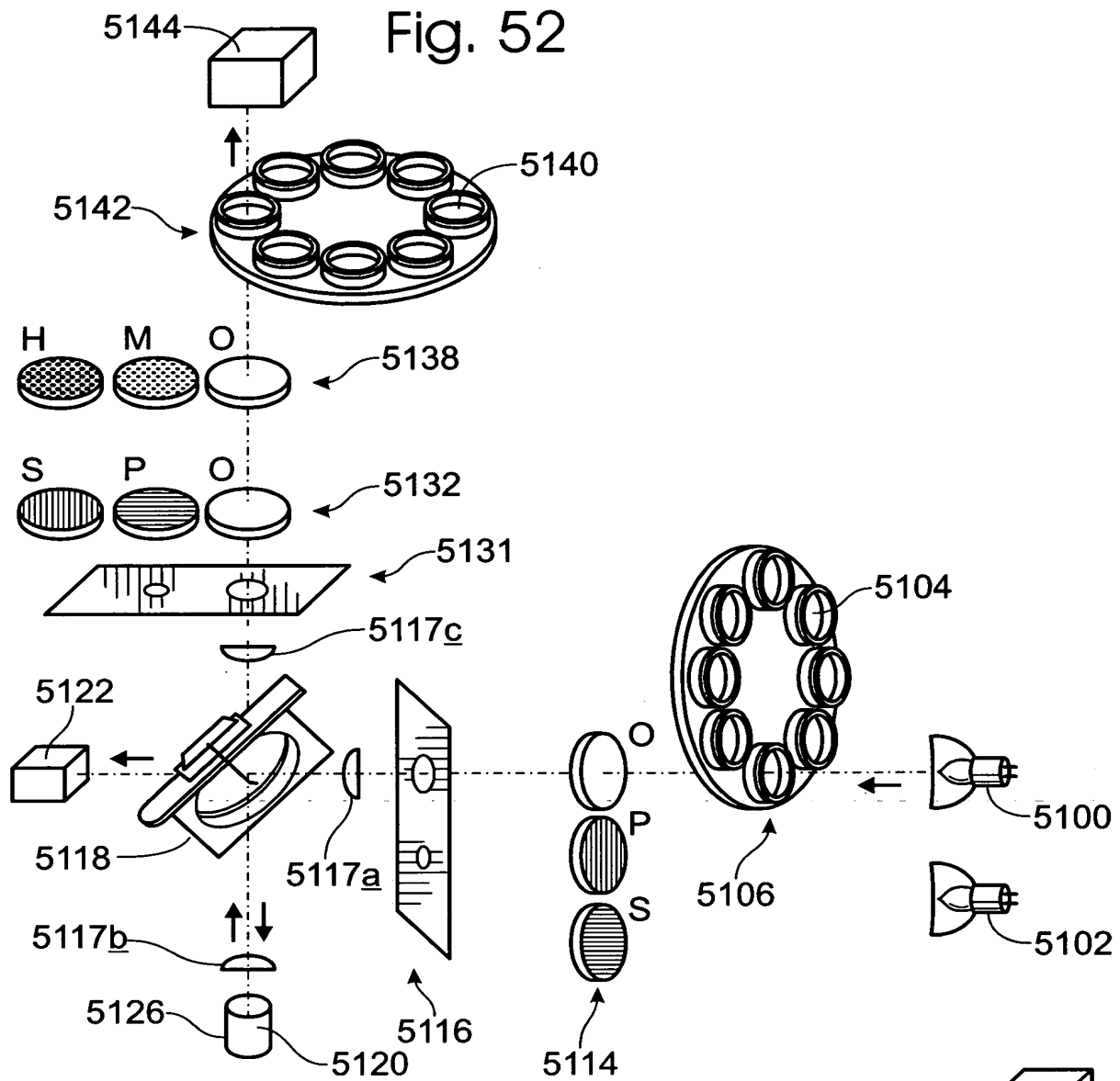


Fig. 53

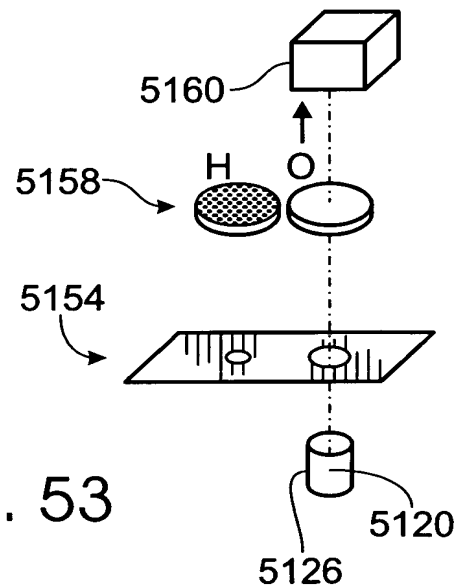


Fig. 54

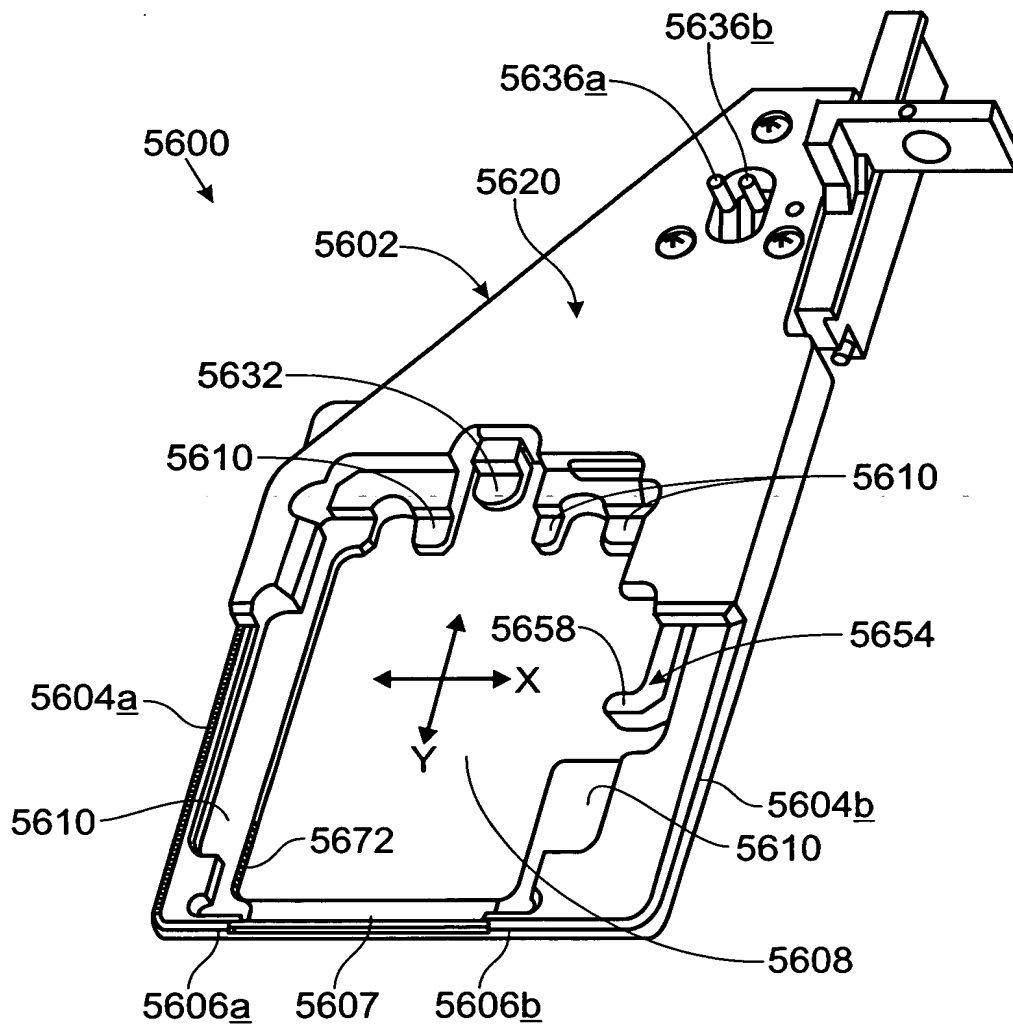


Fig. 55

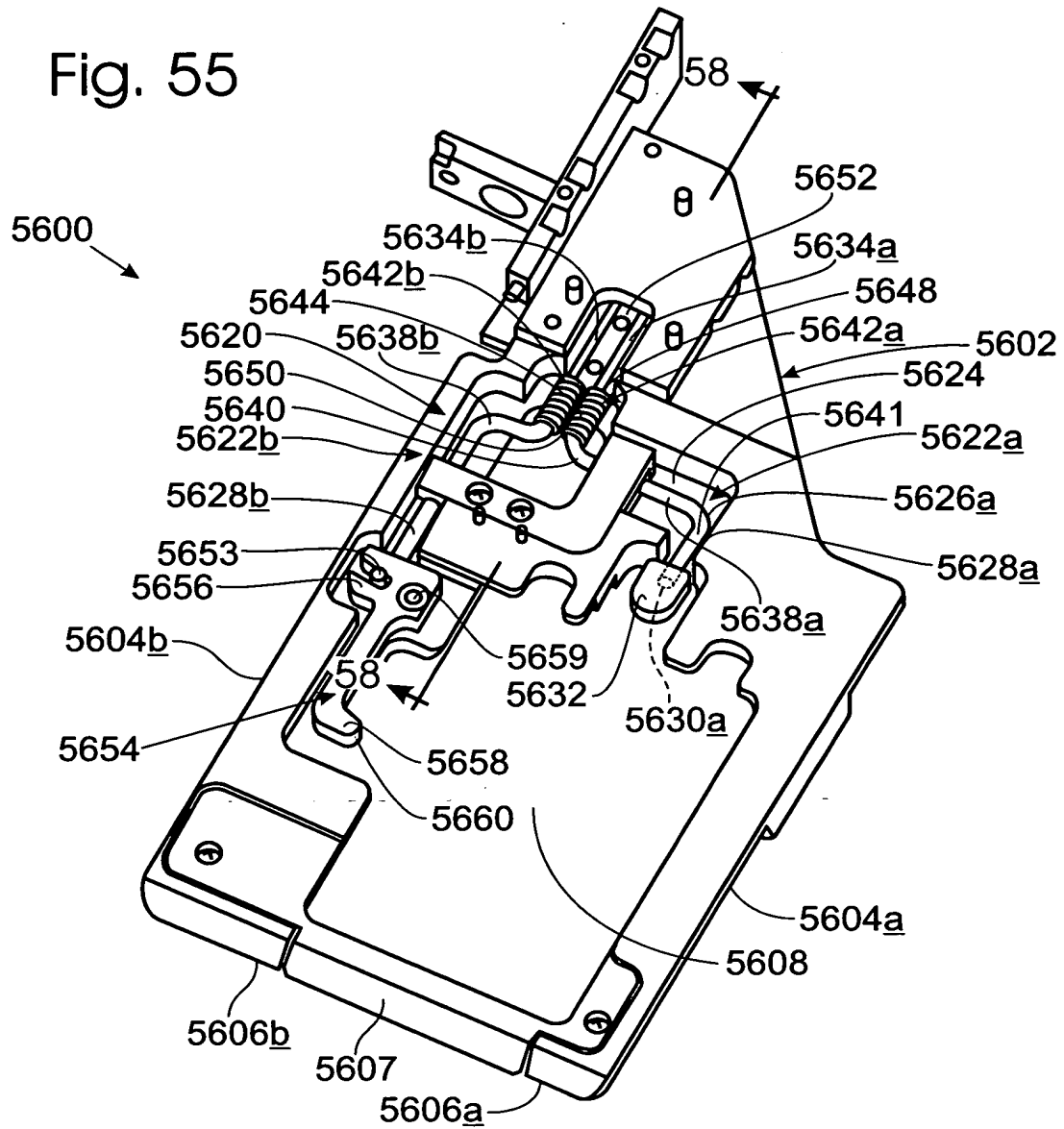


Fig. 56

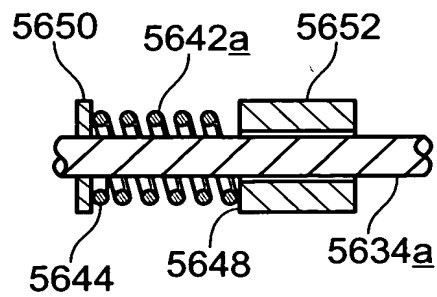


Fig. 57

